Application Report
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Fast Cell Balancing Using External MOSFET

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ABSTRACT

The need for cell balancing comes from the fact that cell-to-cell differences in self-discharge, capacity, and impedance can lead to different charge states among the cells. However, the charger terminates charging based on the summed voltage only, which may leave some cells undercharged and others overcharged. To remedy this imbalance and to achieve the goal of having all cells reaching 100% state-of-charge at charge termination, it is necessary to reduce the charge added to the overcharged cells by creating a current bypass during charging.

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1 Internal Cell Balancing in bq20zxx Solution

The bq20zxx family of gas gauges performs cell balancing using integrated MOSFETs in the analog front end (AFE) ICs (bq29312 for bq20z80, and bq29330 for bq20z70/z90/z75/z95/z40/z45). Figure 1 illustrates two of the four internal cell-balancing channels in the bq29330 AFE. The typical on-resistance of these internal bypass FETs is 330 Ω. (This is assuming only one cell is being balanced; if two adjacent cells are being balanced, typical Rds(on) is 260 Ω, and if three adjacent cells are being balanced, typical Rds(on) is 220 Ω.) The gas gauge circuit uses a set of R-C filters for each of the VCx inputs to suppress noises for the voltage sensing. The typical filter resistor value is 100 Ω. Because the filter resistors are connected in series to the cell-balancing channels, the total bypassing resistance for an active cell-balancing channel is 2 x 100 + 330 = 530 Ω in this example. With a nominal cell voltage of 3.6 V, the cell-balancing current is about 6.8 mA. To balance a cell-to-cell, state-of-charge (SOC) difference of 10% for a 2000-mAh pack, it takes 2000 mAh × 10%/(6.8 mA × D) = 134 hours of charge time (duty cycle D = 0.22 for 2-cell; Table 1 shows the D-value for each device and firmware version), equivalent to a number of charge/discharge cycles. The small cell-balancing current in this configuration may not meet the needs of some applications.

Note: In firmware versions bq20z80 v102, bq20z70 v110, and bq20z90 v110, D is variable, depending on the number of series cells and is 0.4 for 4-cell, 0.3 for 3-cell, and 0.22 for 2-cell. D is a constant value of 0.4 in the latest firmware versions. Use Table 1 to determine the correct D-value based on the device and firmware versions. Also note that bq20z80 v110 and earlier devices (which includes v102) are replaced by bq20z80A v110 and are not recommended for new design (NRND).

Table 1. Select Correct Duty Cycle D-Value

FIRMWARE VERSION	CELL-BALANCING DUTY CYCLE D-VALUE		
	2 SERIES CELLS	3 SERIES CELLS	4 SERIES CELLS
bq20z80 v102 (NRND)	0.22	0.3	0.4
bq20z70 v110	0.22	0.3	0.4
bq20z90 v110	0.22	0.3	0.4
Any future release of z70, z80, and z90	0.4		

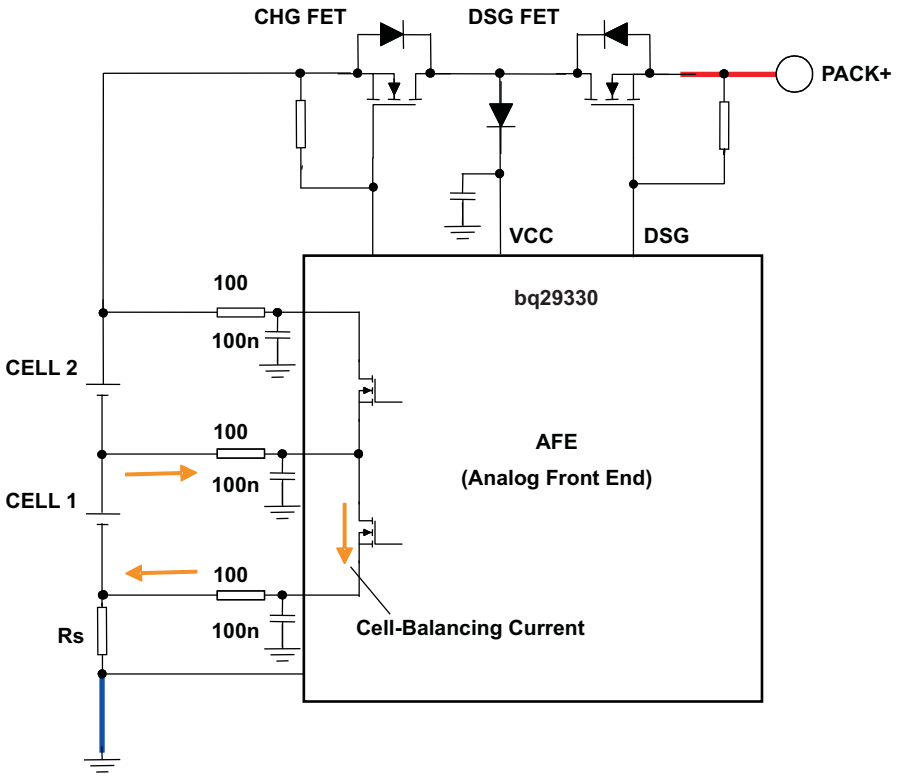

Figure 1. Internal Cell-Balancing Circuit of bq29330 AFE

2 External FET for Accelerated Cell Balancing

Using external MOSFETs to speed up the cell-balancing process by increasing the cell-balancing current is possible. Figure 2 shows the cell-balancing circuit for a 2-cell application. In this circuit, Q1 and Q2 are the external MOSFETs, specifically, Si1034X N-channel dual MOSFETs in a tiny SC-89 package. This FET was chosen because of its low gate-to-source threshold voltage Vgsth. In order to expand the external MOSFET turnon opportunities with varied cell voltages, it is necessary to replace the circuit filtering resistor with 1-kΩ resistor in place of the original 100-Ω value.

Note: The previous edition of this application report indicates that 10 kΩ can be used. Recent study shows that due to the different finite input impedance between each VCx pin, the leakage current at each VCx pin is different. With a 10-kΩ filter resistor, even though the stack voltage can be calibrated accurately, individual cell voltages will not be accurate; the error is typically 10~20 mV. As the Impedance Track™ gauge requires high voltage measurement accuracy for gauging and cell balancing, this error must be minimized. Therefore, the recommended maximum filter resistor value is 1 kΩ, and the resulting voltage error is about 2 mV per cell

When the internal cell-balancing FET is turned on, the two external filter resistors and the Rds(on) of the integrated cell-balancing FET form a resistor-divider, generating a voltage dividing ratio of 0.426 across the 1-kΩ resistor. This is a typical value when cell voltage varies from 3 V to 4.2 V; the ratio can vary between ~0.413 to 0.435 when only a single cell is being balanced. Therefore, if the turnon Vgs for Q1 and Q2 is 1.5 V, for instance, the cell voltage must be higher than 1.5/0.426 = 3.52 V in order for Q1 or Q2 to turn on. For the external, fast cell balancing to work for lower cell voltages, such as the $LiFePO_4$ chemistry, this exercise is especially important. Dual N-channel MOSFETs with lower Vgs thresholds, such as DMN2004DWK, NTZD3154N, and Si1024X, can be considered in this case. Care must be taken to evaluate these devices in terms of maximum Vgsth, absolute maximum rating for Vds and Vgs, and to ensure a drain current of more than 100 mA at low Vgs voltage (such as 1.2 V).

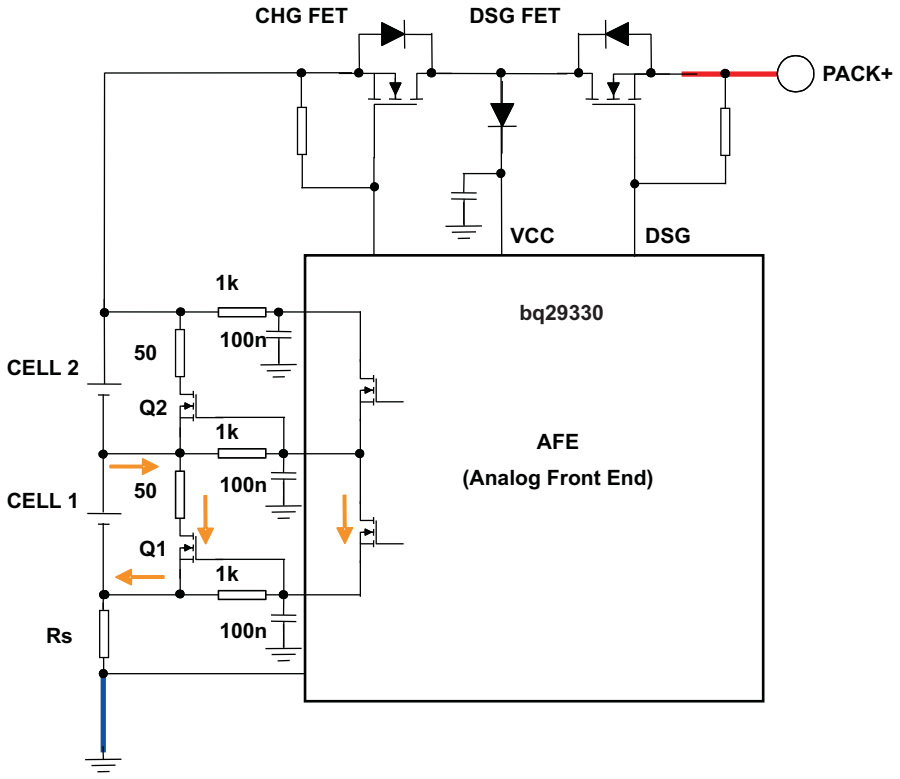

Figure 2. External Cell-Balancing Circuit With Cell 1 Bypassing Active

The operation principle of this circuit is simple. The state of the internal cell-balancing FETs is controlled by the gas gauge. In the circuit of Figure 2, if any internal FET is turned on by the gas gauge, a small current flows from the cathode (the positive tab) of the cell through the top 1-kΩ filter resistor, the internal FET, and the bottom 1-kΩ filter resistor and returns to the anode (the negative tab) of the cell. The two filter resistors and the internal FET on-resistance form a voltage divider, providing the Vgs for the external bypassing FET; the main bypassing current flows through the 50-Ω resistor.

The average on-resistance of Q1, Q2 is about 5 Ω when Vgs ≥ 2 V. With a 50-Ω resistance placed in series with the external MOSFET, the external bypassing path resistance is summed to 55 Ω. At a nominal cell voltage of 3.6 V, the bypassing current is 65 mA. The same calculation for balancing a 10% difference in SOC for a 2000-mAh battery leads to 14 hours of total charge time (using D = 0.22 for a 2-cell battery pack, assuming the use of the bq20z70 v110 firmware).

Note that the bq20zxx gas gauge data flash (DF) constant “Min Cell Deviation” must be calculated and configured based on D and the bypassing current. The DF:MinCellDeviation governs the charging time required to balance the difference of one mAh in cell capacity. The default value of DF:MinCellDeviation is calculated using a nominal voltage of V = 3.6 V, total bypassing R = 700 Ω and duty cycle D = 40% (D = 0.4), and the value is calculated as

DF:MinCellDeviation = R × 3.6/(V × D) = 1750 seconds/mAh, where R is in Ω and V is volts, usually taking a nominal value of 3.6 V.

Applying the same calculation to the external cell-balancing circuit: By using the fast cell-balancing circuit in Figure 2, if the application is a 2-series pack using bq20z70 v110 firmware, D = 0.22 (see Table 1), and R = 50 + 5 Ω, it is necessary to program DF:Min Cell Deviation = 250 seconds/mAh.

Note: The typical Rds(on) of the integrated cell-balancing FET is not a constant value – it is a function of Vds, the drain-to-source voltage of the FET as well as the current through the FET. The higher the cell voltage (and hence the higher the Vds), the lower the Rds(on). Bench measurement of a few bq29330 devices indicates that the typical Rds(on) ranges from 420 Ω (at 3 V) to 300 Ω (at 4.2 V) if **only a single internal cell-balancing FET is turned on at a time**. If multiple adjacent internal cell-balancing FETs are turned on at the same time, Rds(on) is even lower. When balancing two adjacent cells, Rds(on) is ~260 Ω, and when balancing three adjacent cells simultaneously, 220 Ω . For **Internal cell balancing**, it is recommended to use the smallest possible Rds(on), which is 220 Ω, instead of the 500 Ω in the technical reference, when calculating DF:MinCellDeviation.

A demonstration of the circuit was done on two new, 1900-mAh battery cells with a bq20z70 v110 evaluation module. The cells were artificially unbalanced and left sufficiently rested. The open-circuit voltage (OCV) of cell 1 was 3595 mV, corresponding to a state-of-charge (SOC) of 5.6%; the OCV of cell 2 was 3492 mV, corresponding to an SOC of 3.5%. The imbalance in SOC was 5.6% – 3.5% = 2.1%. Then, a charger was applied to the circuit in Figure 2; the [CB] flag was set, indicating that the cell balancing was activated (in this case, the bypassing FET Q2 for cell 1 was turned on). The cell-balancing status is indicated by the orange curve, ChgStat in Figure 3; when ChgStat is high (numerical value 0x240), cell balancing is active. The test charge current is 208 mA. After 2.57 hours, cell balancing was automatically turned off (ChgStat= 0x200) by the gas gauge, indicating that the cell balancing was completed. When the charger was disconnected, the cells were allowed to rest until voltages were stabilized. The resulting voltages were 3784 mV for cell 1 and 3785 mV for cell 2. This test demonstrated that with the fast cell-balancing circuit, a 2.1% SOC deficit of a 1900-mAh cell can be eliminated in 2.57 hours of cell-balancing time. The 1-mV difference between the OCV of the two cells falls within the voltage calibration tolerance. With the internal cell balancing, the bypassed charge in the same time period would have been only 3.2 mAh, less than 0.2% of SOC.

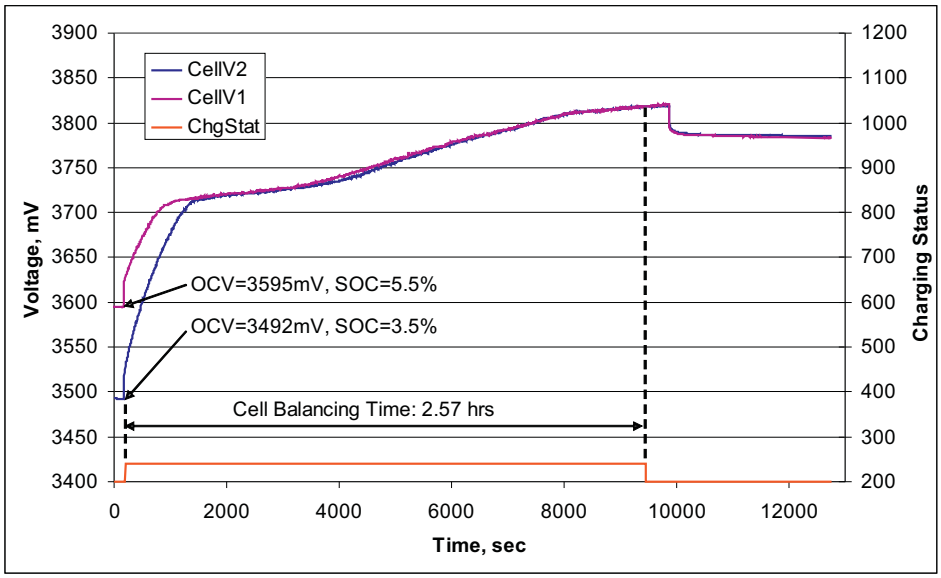

Figure 3. Fast Cell Balancing of Two Series Cells

3 Discussions

Two design aspects are important with the external cell balancing when using the bq29330 or bq29312 AFEs. First, two or three adjacent cells cannot be fast-balanced at the same time. Figure 4a shows the circuit of attempting to balance two adjacent cells simultaneously. When the adjacent internal FETs M1 and M2 are turned on, no current is flowing through Rext2 because Ibias through M1 and M2 cancel at Rext2; therefore, Q2 remains off even when the internal switch M2 is enabled. In practice, it is not an issue because the amount of time required for balancing each cell is evaluated on a per charging-cycle basis by the Impedance Track™ algorithm. Once the balancing of the lower cell is finished, which happens fairly quickly given the fast external balancing, Q2 will be enabled when the gas gauge determines to turn off M1 and keep M2 on. Similarly, in the case when three adjacent cells are simultaneously balanced, the lowest cell of the three is actually balanced first, and then the middle, and lastly the upper one.

The other aspect is the Vds voltage stress when every other cell is being balanced. As illustrated in Figure 4b, the top and the bottom cells are being balanced. Due to the cell-balancing bias, the middle internal switch M2 is seeing a higher Vds, which may exceed the maximum Vds it can sustain. In fact, the Vds of M2 can be calculated based on the worst-case Rds(on) on M1 and M3. Assume that the cells are at approximately 4.2 V, when Rds(on) for M1 and M3 is at the lowest value (about 300 Ω when no adjacent cells are being balanced). Assuming a maximum recommended Rext of 1 kΩ, Vds of M2 can be as high as 4.2 V + 2 x 4.2 x 1000/(2 x 1000 + 300) = 7.85 V. The maximum Vds under this setting is still below the absolute maximum value of 8.5 V for the internal balancing FETs; so, this is fine. Apparently, with higher Rext, Vds stress seen by M2 can be worse and can even exceed the maximum voltage. This is another reason that the maximum recommended Rext is 1 kΩ.

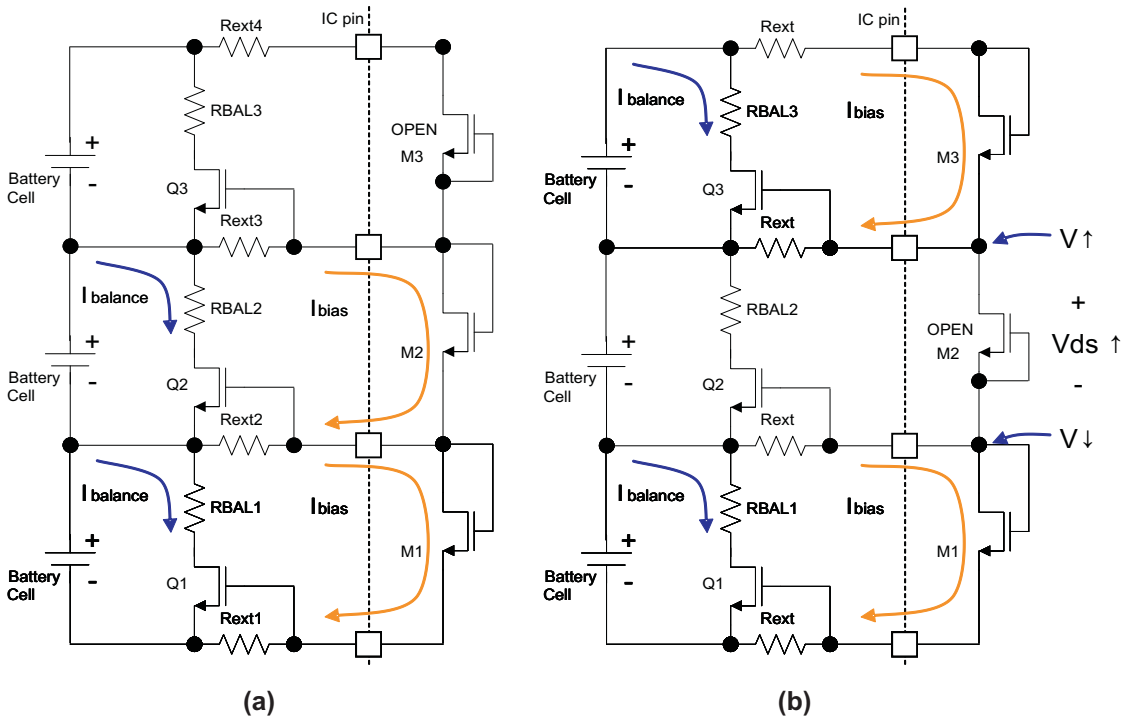

Figure 4. Issues With Balancing Two Adjacent Cells (a) and Every Other Cell (b)

4 Summary

This application report documents a fast cell-balancing circuit using existing bq29330/bq29312 AFE for bq20z80/z70/z90/z75/z95 Impedance Track™ gas gauges and a couple of various design aspects when implementing this circuit.

5 Acknowledgment

This application report has adopted results from some insightful discussions with Lon Schneider, Nexergy, Inc.

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