Application Note

How to use the BQ25970 for Flash Charging

Xiaohu Qin, Alen Chen

ABSTRACT

In smartphone applications, end users are always pursuing a faster and cooler charging experience, so the smartphone designer has to face more challenges than before. Texas Instruments released the new generation Flash Charger, BQ25970, to help smartphone designers meet these targets easily. The BQ25970 device can support from 20 W up to 50 W with a typical 97% efficiency with standalone or parallel configuration to provide a better user experience.

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Trademarks

1 Introduction

1.1 Key BQ25970 Specifications

The BQ25970 has the following specifications:

- 97% Efficient power stage for 8-A fast charge
- Switched capacitor architecture optimized for 50% duty cycle:
  - Input voltage is 2 × battery voltage (3.5 V to 4.65 V)
  - Output current is 2 × of input current (up to 4.5 A)
  - Reduces power loss across the cable
- Integrated programmable protection features for safe operation
  - Input overvoltage protection (BUS_OVP)
  - Input overcurrent protection (BUS_OCP) with adjustable alarm
  - Input overvoltage with external OVP FET (VAC_OVP up to 17 V, bq25970 only)
  - Battery overvoltage protection (BAT_OVP) with adjustable alarm
  - Output overvoltage (VOUT_OVP)
  - Input overcurrent protection (BUS_OCP) with adjustable alarm
  - IBAT overcurrent protection (BAT_OCP) with adjustable alarm
  - Battery temperature monitoring
  - Connector temperature monitoring
- Integrated 12-bit effective analog-to-digital converter (ADC)
  - ±0.5% BUS voltage
  - ±0.5% VOUT voltage
  - –0.4% to 0.2% BAT voltage with differential sensing
  - ±1.5% BAT current at 6 A with External R_{SENSE}
  - ±1% BAT temperature
  - ±1% BUS temperature
  - ±4°C Die temperature

1.2 BQ25970 Simplified Power Stage

The BQ25970 device adopts charge pump topology with a 2-phase interleaving fixed 50% duty-cycle, this structure can get higher efficiency because the 2-phase power stage can balance power dissipation between them.

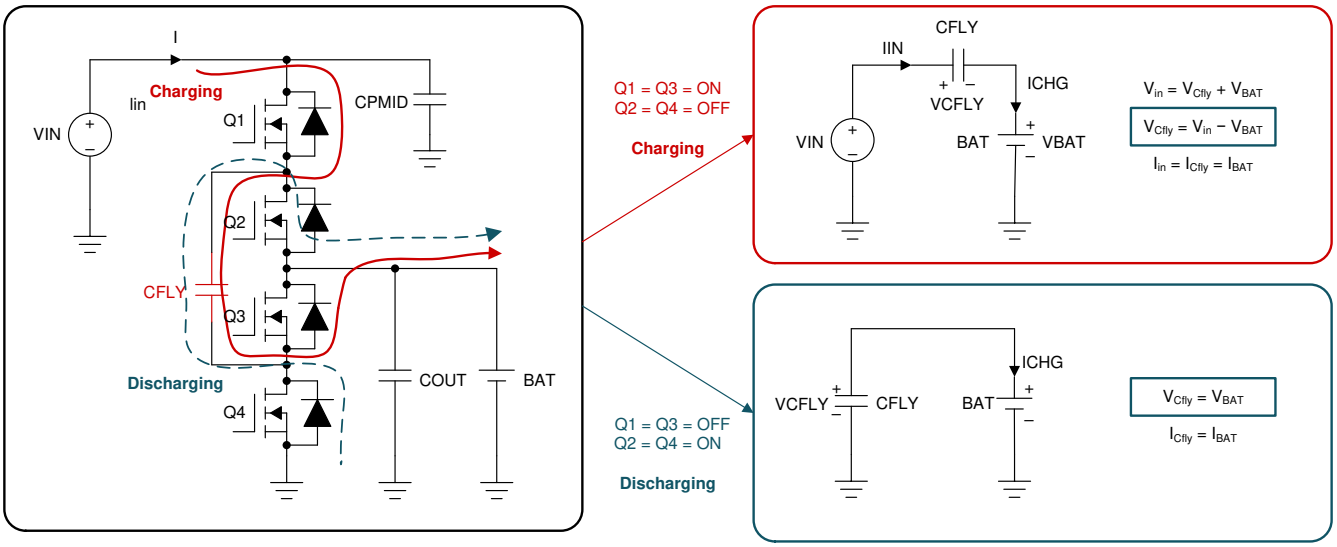

Figure 1-1. Ideal Charge Pump Working Process

Based on the ideal (ignore all of the impendence on power stage and power trace) working process of a charge pump as Figure 1-1 shows, the equation between V_{IN} and V_{BAT} can be expressed as,

$$V_O = V_{BAT} = \frac{1}{2} \times V_{IN} \quad (1)$$

Equation 1 shows V_O is always following V_{IN}, in other words, the BQ25970 device behaves just like a kind of 2:1 voltage follower, when V_{IN} changes, V_O is changed accordingly.

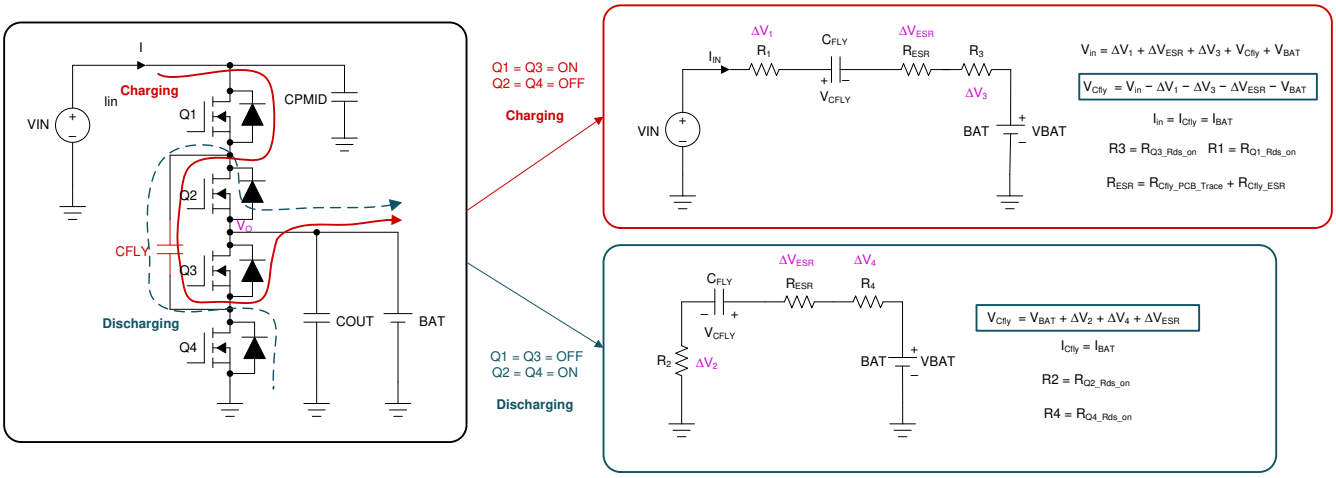

Figure 1-2. Actual Charge Pump Working Process

In an actual system, the impedance on the power stage and power trace cannot be ignored, as Figure 1-2 shows. The internal resistance of the BQ25970 device can be described as R1 –R4 or $R_{DS(on)}$ for Q1–Q4, R_{ESR} means CFLY capacitor ESR, so change Equation 1 as in Equation 2:

$$V_{BAT} = \frac{1}{2} \times \left(V_{IN} - \Delta V2 - \Delta V4 - \Delta V1 - \Delta V3 - 2 \times \Delta V_{ESR} \right) \quad (2)$$

Some definitions can be made in the whole working cycle of the charge pump, charging and discharging as done in Equation 3, and Equation 4.

$$\Delta V_{BQ25970\_SYS} = \Delta V2 + \Delta V4 + \Delta V1 + \Delta V3 + 2 \times \Delta V_{ESR} \quad (3)$$

$$R_{BQ25970\_SYS} = R2 + R4 + R1 + R3 + 2 \times R_{ESR} \quad (4)$$

Then, substitute $\Delta V_{BQ25970\_SYS}$ into the original formula:

$$V_{BAT} = \frac{1}{2} \times \left(V_{IN} - \Delta V_{BQ25970\_SYS} \right) \quad (5)$$

This reforms Equation 5 into Equation 6,

$$V_{IN} = 2 \times V_{BAT} + \Delta V_{BQ25970\_SYS} \quad (6)$$

Since the BQ25970 device is a 2:1 charge pump, V_O will be expressed as Equation 7.

$$V_O = \frac{1}{2} \times V_{IN} = \frac{1}{2} \times \left(2V_{BAT} + \Delta V_{BQ25970\_SYS} \right) = V_{BAT} + \frac{1}{2} \Delta V_{BQ25970\_SYS} \quad (7)$$

To create a charger using a Programmable Power Supply (PPS) protocol, such as the Power Delivery (PD) protocol, use an output voltage set slightly higher (such as ΔV) than 2 times the calculated voltage, as in Equation 7, (V_{BAT} + 0.5 × $\Delta V_{BQ25970\_SYS}$). To the BQ25970 device, it does not have a feedback loop for V_O, therefore, it is a kind of open loop power source, meaning that the BQ25970 device should be looked upon as a power source with non-zero internal resistance because its output voltage cannot be kept to a fixed value (for a power converter with feedback control loop, because the control loop can always keep the output as a fixed value whatever load current changes or not, meaning its internal resistance can be looked as 0, or an ideal power source). As Figure 1-3 shows, it is equivalent V_{O_PPS} circuitry for BQ25970 output, it can be viewed as an ideal power source with internal resistance: the internal resistance is $R_{BQ25970\_SYS}$, the voltage of $V_{O\_PPS\_Ideal}$ equals to V_{O_PPS} from the PPS pre-set according to PPS protocol and all of impendence on the BQ25970 and PCB trace is ignored.

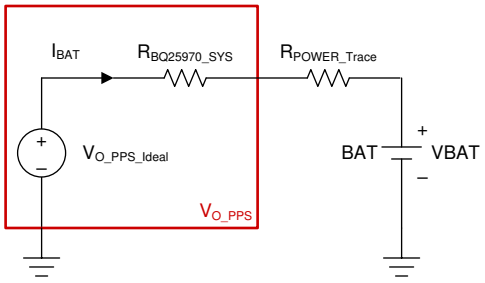

Figure 1-3. V_{O_PPS} Equivalent Circuitry

$$V_{IN\_PPS} = 2 \times \left(V_{BAT} + \frac{1}{2} \times \Delta V_{BQ25970\_SYS} \right) + \Delta V \tag{8}$$

$$V_{O\_PPS} = \frac{1}{2} \times V_{IN\_PPS} = V_{BAT} + \frac{1}{2} \times \Delta V_{BQ25970\_SYS} + \frac{1}{2} \times \Delta V \tag{9}$$

Equation 8 and Equation 9 assumes the total resistance of power trace between BQ25970 output and battery is R_{Power_Trace}, the charging current is calculated using Equation 10:

$$I_{BAT} = \frac{V_{O\_PPS} - V_{BAT}}{R_{BQ25970\_SYS} + R_{Power\_Trace}} = \frac{\frac{1}{2} \times \left(\Delta V_{BQ25970\_SYS} + \Delta V \right)}{R_{BQ25970\_SYS} + R_{Power\_Trace}} \tag{10}$$

Note

For a detailed description of R_{Power_Trace}, see Section 3.2.

In Equation 10, either ΔV or R is changed and the charging current will be changed accordingly. If the designer can keep R or ΔV on power trace at a lower level, they will get higher efficiency at the same charging current condition.

2 PPS Protocols for BQ25970

2.1 What is the PPS Protocol?

PPS Protocol is a dedicate protocol for power sources, it can be used to adjust output voltage or current of power supplies according to system commands or system requests. In other words, it makes a power source more intelligent and the system can control the power source freely, such as output current, output voltage, total output capability , and so forth. All control of information can be added into PPS protocol. Any devices that comply with PPS protocol can decode it and communicate each other smoothly to attain the expected voltage or current.

2.2 PPS Protocol Working Process Sample

Generally, in an actual system, PPS protocol is always running in the AP (Application Processor) or PMU (Power Management Unit) side, which means that the PPS protocol is independent of the BQ25970 device. All decoding processes about PPS protocol, such as PD3.0, take place in AP or PMU. To designers, it is very flexible, they can run any PPS protocols (standard or customized) in AP or PMU to realize fast charging functions. In Figure 2-1, the host device is a smartphone and the slave device is an AC adaptor. The smartphone sends a command to the AC adaptor, and the AC adaptor will response to the smartphone command and adjust the output voltage or output current.

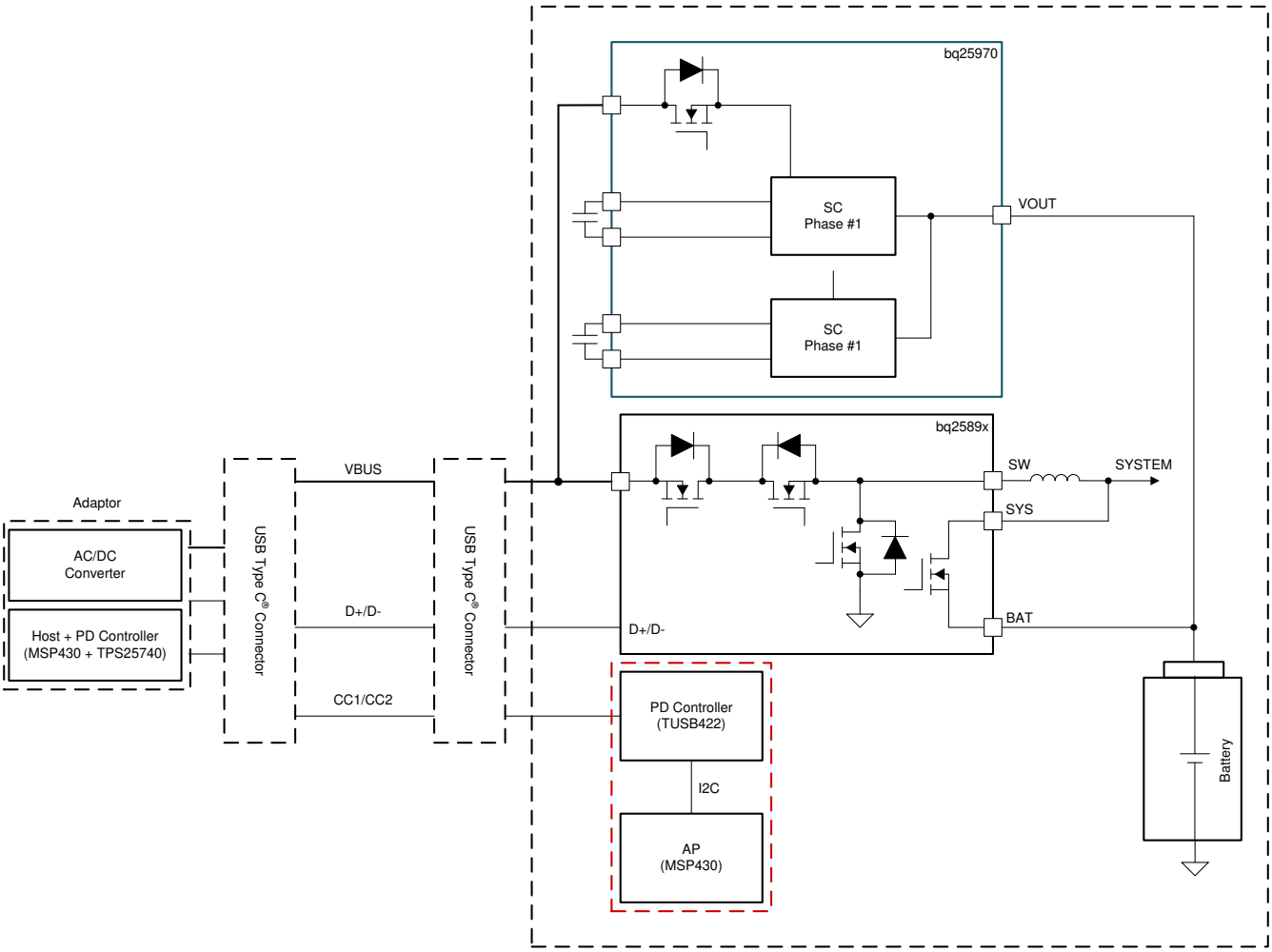

Figure 2-1. PPS Working Process

The PPS protocol decoding unit is marked with a red line as Figure 2-1 shows. Of course, in a real smartphone system, this unit will be replaced by AP/PMU. In Figure 2-1, PPS protocol is PD3.0 and it is done using TI's MCU MSP430 The TUSB442 device, also from TI, is a USB Type-C™ PD controller that can communicate with an AC adaptor with PD3.0 protocol. When the PD AC adaptor is plugged into a smartphone, the AP will handshake with the AC adaptor by toggling the CC pin. After initial communication, the smartphone recognizes the AC adaptor and sends a PD command to the AC adaptor, after that the AC adaptor responds to the smartphone and the output target voltage and current as the smartphone sends requests to start the flash charging process. During the charging, the BQ25970 device will be always reporting battery voltage and charging current status to the AP. According to the BQ25970 continuous reporting, the AP will keep updating new commands to the AC adaptor to adjust the output voltage or current so as to keep constant current charging process until finishing the flash charging stage.

3 Key Design Tips for BQ25970

3.1 Simplified Schematic

Figure 3-1 illustrates the BQ25970 simplified schematic.

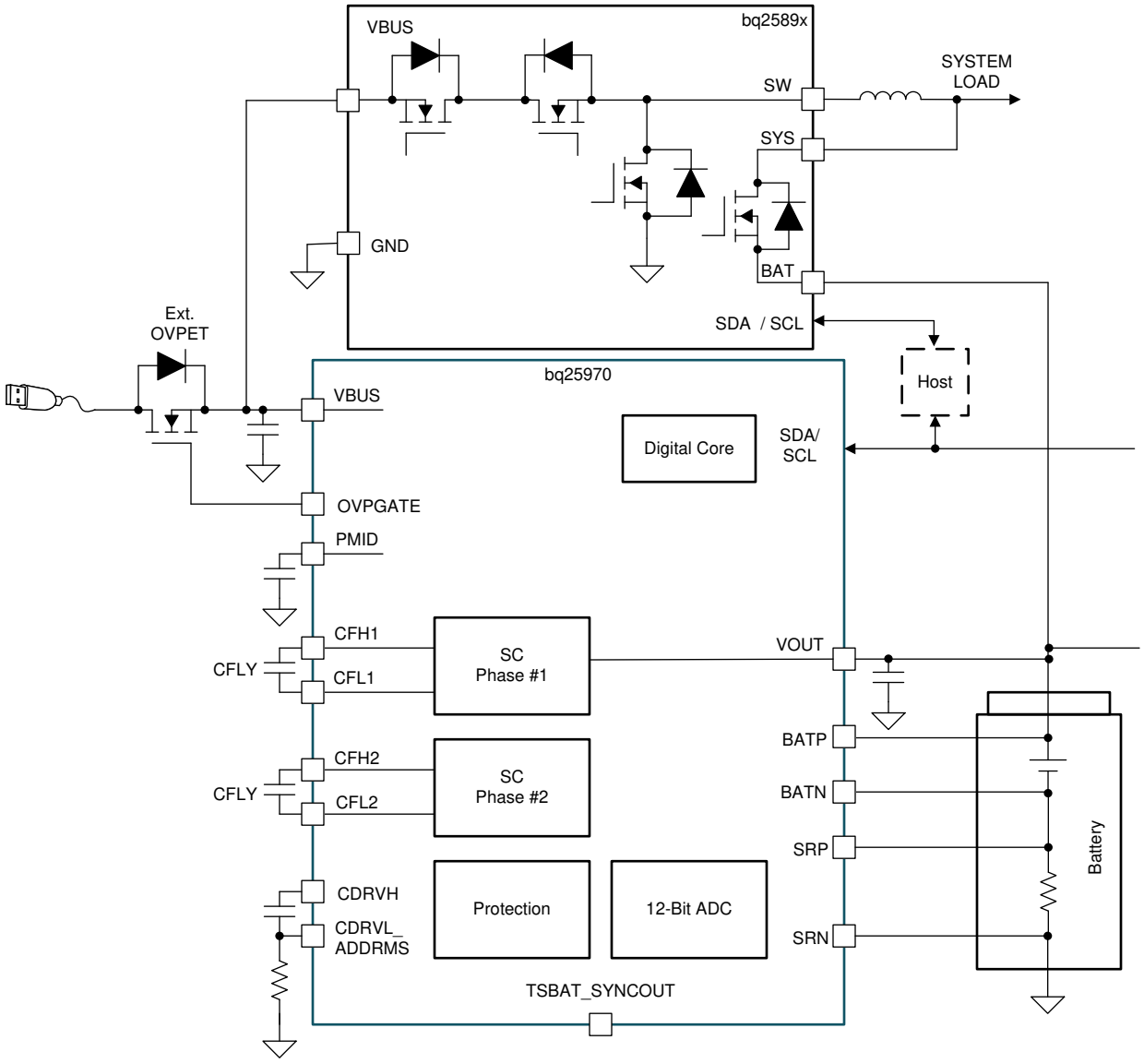

Figure 3-1. BQ25970 Simplified Schematic

- CFLY is charge pump capacitor, it is a power storage component
- The external MOSFET is used for overvoltage protection of VBUS and it can replace the dedicated OVP switch in VBUS with a low-cost MOSFET

In general, all power capacitors for BQ25970 applications should be MLCC (Multiple Layer Ceramic Capacitor) because of their smaller package, lower ESR, and lower power dissipation. The biggest shortfall of a MLCC is that the effective capacitance is derated due to DC biased voltage on the capacitor. When DC biased voltage on the MLCC increases, the effective capacitance of the MLCC will decrease accordingly. It is necessary to keep enough capacitance, in an actual design, the DC biased voltage curve vs. capacitance in the MLCC data sheet is a useful tool to find a suitable power capacitor. As Figure 3-2 shows, when DC biased voltage increases, the effective capacitance decreases quickly. Of course, the designer has to consider whether the maximum voltage that the power capacitor supports can meet an actual request. For example, if the power rail is 10 V, then the designer should choose a 16-V MLCC to avoid any failures . Meanwhile, the designer has to consider the impact

of temperature on the effective capacitance because different ambient working temperatures will lead to the change of effective capacitance.

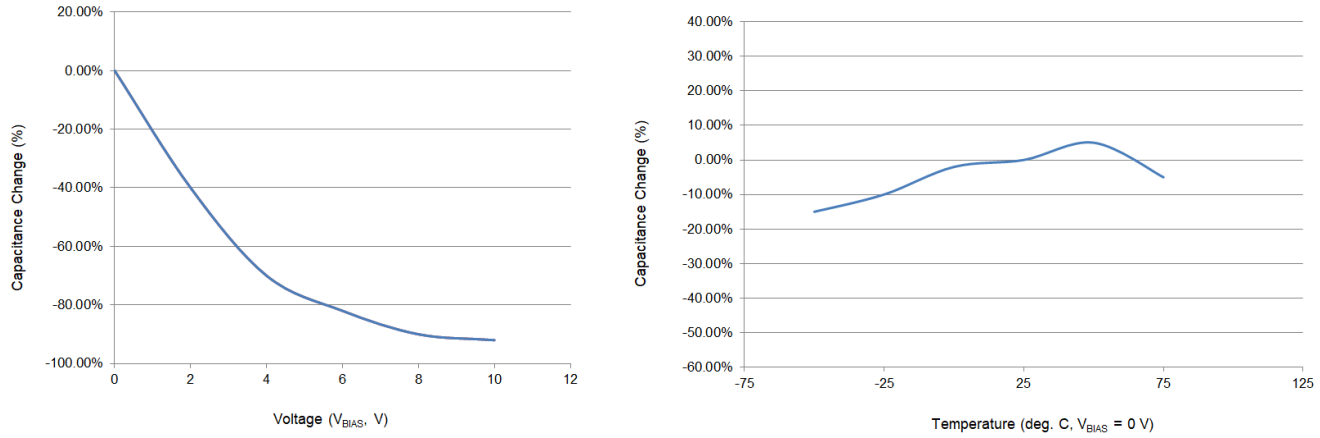

Figure 3-2. MLCC Effective Capacitance vs DC Biased Voltage and Temperature

The external MOSFET will act as an OVP function, so when choosing a MOSFET, its maximum rating voltage of V_{DS} is important. It depends on the maximum voltage on VBUS, when the voltage on VBUS exceeds the OVP setting of the BQ25970 device, this MOSFET will be turned off immediately, typically in less than 100 ns. Also, the $R_{DS(on)}$ of the MOSFET will impact efficiency, so a lower $R_{DS(on)}$ MOSFET is a good choice. Finally, the V_{GS} of the MOSFET should be more than 10 V.

The MOSFET CSD17577Q3A specification table in (Figure 3-3) from the *CSD17577Q3A 30-V N-Channel NexFET™ Power MOSFET* data sheet shows: key parameters, V_{DS}, $R_{DS(on)}$, and V_{GS}.

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	12		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.5		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	5.3	mΩ
		V_{GS} = 10 V	4.0	mΩ
$V_{GS(th)}$	Threshold Voltage	1.4		V

Ordering Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17577Q3A	2500	13-Inch Reel	SON 3.3 × 3.3 mm Plastic Package	Tape and Reel
CSD17577Q3AT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	35	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	83	
	Continuous Drain Current (1)	19	
I_{DM}	Pulsed Drain Current (2)	239	A
P_D	Power Dissipation(1)	2.5	W
	Power Dissipation, T_C = 25°C	53	
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 28 A, L = 0.1 mH, R_G = 25 Ω	39	mJ

Figure 3-3. MOSFET Key Specification Table

3.2 How to Translate R on Power Trace From input to Output of BQ25970 or Reversely

As previously described, the BQ25970 device acts like a 2:1 converter, so it can be expressed with an equivalent transformer model as this section shows.

$$V_{IN} = 2 \times V_O \tag{11}$$

$$I_{IN} = \frac{1}{2} \times I_O \tag{12}$$

Using the same theory, Equation 13 is a re-expression of Equation 11 and Equation 12.

In Equation 13, ΔV_X means the voltage drop on the power trace.

$$\Delta V_{IN} = 2 \times \Delta V_O \tag{13}$$

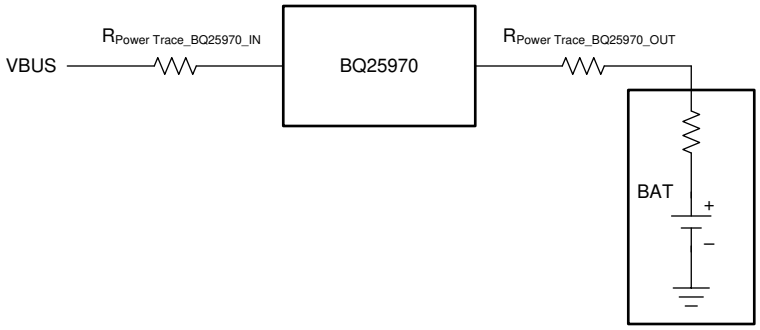

Figure 3-4. R on Power Trace Translation

R translation from output to input:

Assumes that the output power trace resistance of BQ25970 is $R_{Power\ Trace\_BQ25970\_OUT}$ as Figure 3-4 shows.

This can also be represented as shown in Equation 14.

$$R_{Power\ Trace\ BQ25970\_OUT} = \frac{\Delta V_O}{I_O} \tag{14}$$

Equation 15 is an example when converted to the input resistance of the BQ25970 device.

$$R_{Power\ Trace\ BQ25970\_IN} = \frac{\Delta V_{IN}}{I_{IN}} = \frac{2 \times \Delta V_O}{\frac{1}{2} \times I_O} = 4 \times R_{Power\ Trace\ BQ25970\_OUT}$$

$$R_{Power\ Trace\ BQ25970\_IN} = 4 \times R_{Power\ Trace\ BQ25970\_OUT} \tag{15}$$

R translation from input to output:

In the same way, assumes that the input power trace resistance of the BQ25970 device is $R_{Power\ Trace\_BQ25970\_IN}$ as Figure 3-4 shows.

This can also be represented as shown in Equation 16.

$$R_{Power\ Trace\ BQ25970\_IN} = \frac{\Delta V_{IN}}{I_{IN}} \tag{16}$$

Equation 17 is an example when converted to the output resistance of the BQ25970 device,

$$R_{Power\ Trace\ BQ25970\_OUT} = \frac{\Delta V_O}{I_O} = \frac{\frac{1}{2} \times \Delta V_{IN}}{2 \times I_{IN}} = \frac{1}{4} \times R_{Power\ Trace\ BQ25970\_IN} \tag{17}$$

$$R_{Power\ Trace\_BQ25970\_OUT} = \frac{1}{4} \times R_{Power\ Trace\_BQ25970\_IN} \tag{18}$$

Designers can easily evaluate the power dissipation in different power traces to improve thermal performance by using Equation 15 or Equation 18. Also, the BQ25970 device supports parallel configuration to get much higher charging current, such as 10 A or more. This method can help the designer to optimize the PCB layout of power trace and get almost the same charging current between two BQ25970 devices to get excellent thermal performance.

3.3 PCB Layout Tips for BQ25970

Proper PCB layout ensures good performance, so the designer must pay attention on PCB layout as the PCB layout sample in Figure 3-5 shows.

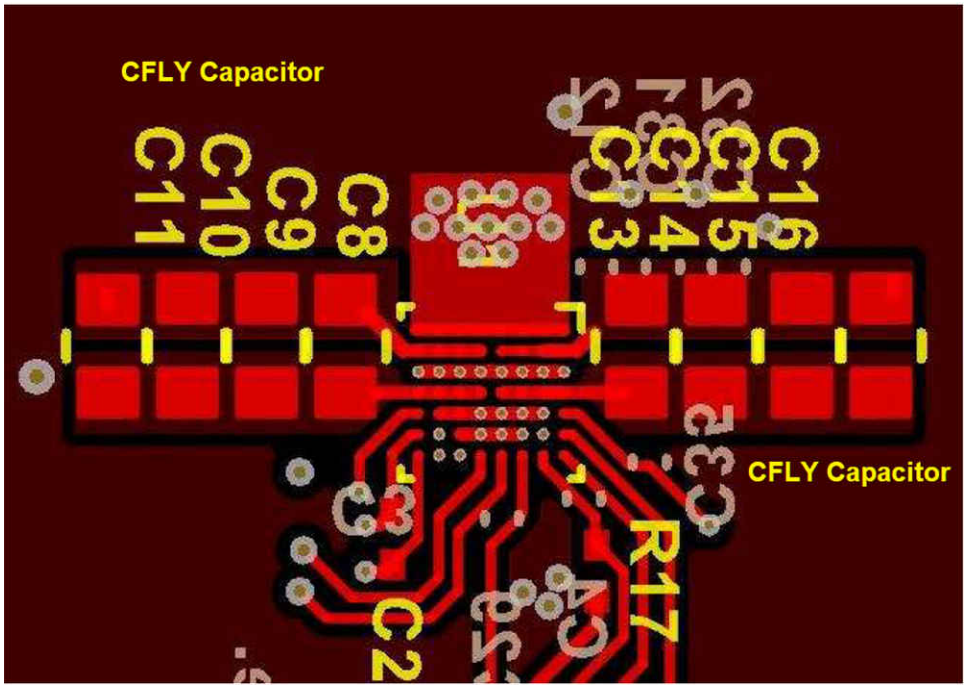

Figure 3-5. BQ25970 PCB Layout

- CFLY capacitors are placed close to the BQ25970 device, the power trace should be short and wide to decrease power loss on the PCB trace.
- Connect the GND pin to the main ground plane directly to get better thermal sink and better EMI performance.
- The width of the external MOSFET gate driving trace between the OVPGATE pin and the external MOSFET gate should be 10 mil or more because of high di/dt when OVPGATE is active. Also, it is better to surround this driving trace with a ground wire to avoid any noise interference.
- The battery sense trace BATP and BATN should be routed as differential traces, and connect them to the battery socket terminal directly. If possible, surround them with ground trace to avoid noise interference.

4 References

- Texas Instruments, *bq25970, bq25971 I²C Controlled Single Cell High Efficiency 8-A Switched Cap Fast Chargers With ADC Data Sheet*
- Texas Instruments, *bq25970 PWR893 Evaluation Module User's Guide*

5 Revision History

Changes from Revision * (March 2020) to Revision A (October 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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