Application Report
SLVA489–November 2011

Voltage Margining Using the TPS62130

Darwin Fernandez *PMP- Portable Power*

ABSTRACT

Voltage margining is a means of verifying the robustness of a product by intentionally adjusting its supply voltages to their limits and then evaluating the product's performance to ensure that it still meets its specifications at the power supply's extremes. The TPS62130 synchronous step-down dc-dc converter features an integrated output voltage scaling function that allows for +5% margining by use of its DEF pin. This application report demonstrates a simple circuit that provides –5% margining to complete a ±5% margining function. This permits testing for high- and low-voltage margining for product evaluation. This application circuit can be used with any of the TPS62130, TPS62140, and TPS62150 devices.

1 Introduction

Voltage margining is the process of dynamically testing a load circuit over its supply voltage range. This evaluates the load circuit's ability to tolerate changes in the power supply voltages that may occur over time and temperature. The testing is typically performed by forcing the power supply to ±5% of its nominal output voltage and then ensuring that the end-equipment still passes its final acceptance test.

2 TPS62130 DEF Pin Operation

The TPS62130 is a high-frequency, synchronous, step-down, dc-dc converter optimized for high power density applications. A special feature of the TPS62130 is its integrated output voltage scaling function that allows for +5% margining by use of the DEF pin as described in Table 1. When the DEF pin is pulled low, the power supply's output voltage is regulated to its nominal value. When the DEF pin is pulled high, the power supply's output voltage increases to its nominal voltage +5%.

Table 1. DEF Pin Functionality

Input	Output Voltage
Low (0)	Nominal
High (1)	Nominal +5%

3 Using the TPS62130 for Voltage Margining

A simple circuit is added to provide a –5% voltage margining function. Adding a series resistor and switch in parallel with the bottom FB pin resistor, R2, allows the output voltage to be increased when the added resistor, R3, is switched into the FB divider. Figure 1 shows the TPS62130EVM-505 with the added -5% voltage margining circuit (R3, R4, and SW1).

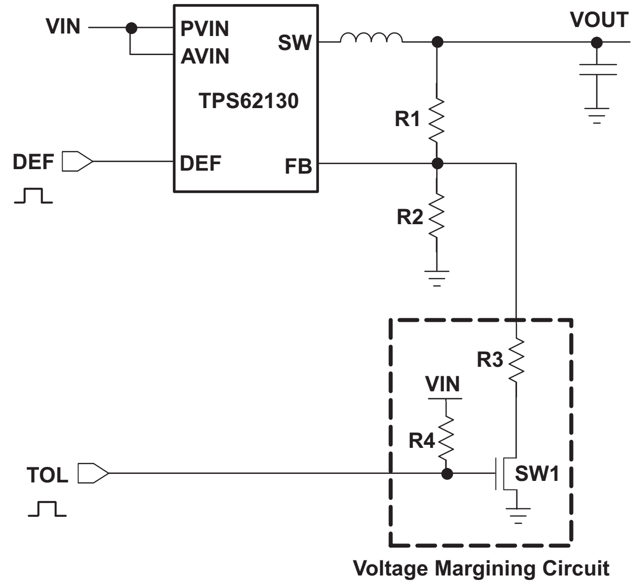


Figure 1. TPS62130 With –5% Voltage Margining Circuit

Initially, R1 and R2 are set to yield an output voltage equal to the nominal voltage –5%. As a result, when SW1 is opened, the output voltage equals the nominal voltage –5%. When SW1 is closed, R2 and R3 are in parallel. This changes the effective resistance of the feedback network so that the output voltage equals its nominal voltage. When the DEF pin is set to a logic high, the output voltage increases to its nominal voltage +5%. Thus, the TOL and DEF signals combine to create ±5% margining, as shown in Table 2.

Table 2. Voltage Margining Using the DEF and TOL Signals

DEF	TOL	Output Voltage
0	0	Nominal –5%
0	1	Nominal
1	0	Nominal
1	1	Nominal +5%

During normal operation, the default operation of this circuit sets the output voltage to its nominal value with DEF low and TOL high. To achieve this configuration simply, both DEF and TOL may be left floating with DEF pulled down by the internal resistor on that pin and TOL pulled high by R4.

4 Design Considerations

Resistor R2 is chosen, as described in the TPS62130 data sheet (SLVSAG7), and must not exceed approximately 400 kΩ.

Resistor R1 is chosen using Equation 1 under the condition that R1 + R2 does not exceed 2 MΩ:

$$R1 = R2\left(\frac{V_{nominal} - 5\%}{0.8} - 1\right) \quad (1)$$

If R1 + R2 exceeds 2 MΩ, reduce the value of R2 and repeat Equation 1. Resistor R3 is chosen using Equation 2.

$$R3 = \frac{R' \times R2}{R2 - R'} \quad \text{where} \quad R' = \frac{R1}{\frac{V_{nominal}}{0.8} - 1} \quad (2)$$

Resistor R4 is a pullup resistor. Its value is not critical to the circuit’s operation. For simplicity, its value is chosen to be the same as R3.

Switch SW1 is an NMOS transistor and must have a gate-to-source rating in excess of the maximum input voltage and have a drain-to-source rating exceeding the output voltage. If an NMOS with a lower gate to source rating is desired, a resistor must be added from gate to ground to reduce the voltage on the gate.

5 Design Example

The following margining conditions were implemented using the TPS62130EVM-505.

- Vout nominal = 3.3 V
- Vout – 5% = 3.135 V
- Vout + 5% = 3.465 V

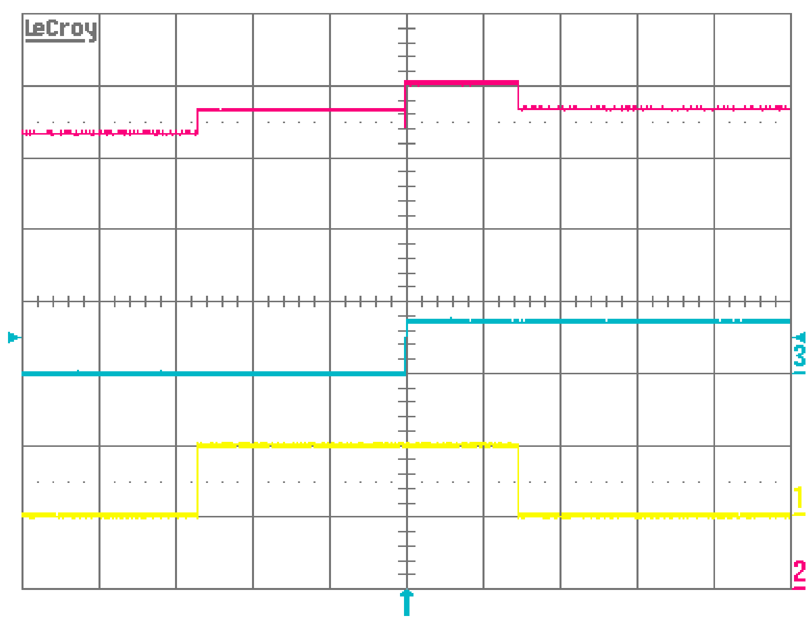
Using the design equations in the previous section, R1, R2, R3, and R4 are calculated. Table 3 shows the calculated values and the actual resistor values implemented in the design.

Table 3. Resistor Values Calculated and Actual

Resistor	Calculated (kΩ)	Actual (kΩ)
R1	219	215
R2	75	75
R3	832	825
R4	832	825

An NMOS switch that satisfies this application is the 2SK3019.

Figure 2 shows resulting waveforms that the voltage margining circuit produces. Initially, the DEF and TOL signals are low, making the output voltage 3.135 V (nominal – 5%). When the TOL signal is high and DEF pin low, the output voltage is 3.3 V (nominal). Then, when the TOL signal and DEF pins go high, the output voltage is 3.465 V (nominal +5%). Lastly, DEF is high and TOL is low, resulting in the nominal output voltage again.



200 ms/div

Pink = Vout 0.5 V/div
Blue = DEF 5 V/div
Yellow = TOL 5 V/div

Figure 2. TPS62130 Voltage Margining Using the DEF and TOL Signals

A 100-mA load was added during this test to pull down the output voltage when the voltage was lowered in the last step. Because the TPS62130 does not actively source energy from the output back to the input, the output voltage only decreases due to the load and/or leakage paths on the output. Without a load, the output voltage might decrease slower.

6 Conclusion

This application report demonstrates a simple circuit that allows voltage margining on the output of the power supply using the DEF function of the TPS62130 and an additional TOL signal. This allows evaluation of product performance at the limits of the power supply voltage.