Application Report
SLVA478B –September 2011–Revised October 2013

Using the TPS62120 in an Inverting Buck-Boost Topology

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ABSTRACT

The TPS62120 is a synchronous buck dc-to-dc converter designed for low-power applications. It features a wide operating input voltage range from 2 V to 15 V, up to 96% efficiency, and 75-mA output current. This device family is well-suited for many applications such as ultra low-power microprocessors, energy harvesting, and low-power RF applications. Moreover, the TPS62120 can be configured in an inverting buck-boost topology, where the output voltage is inverted or negative with respect to ground. This application note describes the TPS62120 in an inverting buck-boost topology for use in low current negative rails for operational amplifier biasing and other low-power applications. This document also applies to the TPS62122.

Contents

List of Figures

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1 Inverting Buck-Boost Topology

1.1 Concept

The inverting buck-boost topology is very similar to the buck topology. In the buck configuration shown in Figure 1, the positive connection (VOUT) is connected to the inductor and the return connection is connected to the integrated circuit (IC) ground. However, in the inverting buck boost configuration shown in Figure 2, the IC ground is used as the negative output voltage pin (labeled as –VOUT). What used to be the positive output in the buck configuration is used as the ground (GND). This inverting topology allows the output voltage to be inverted and is always lower than the ground.

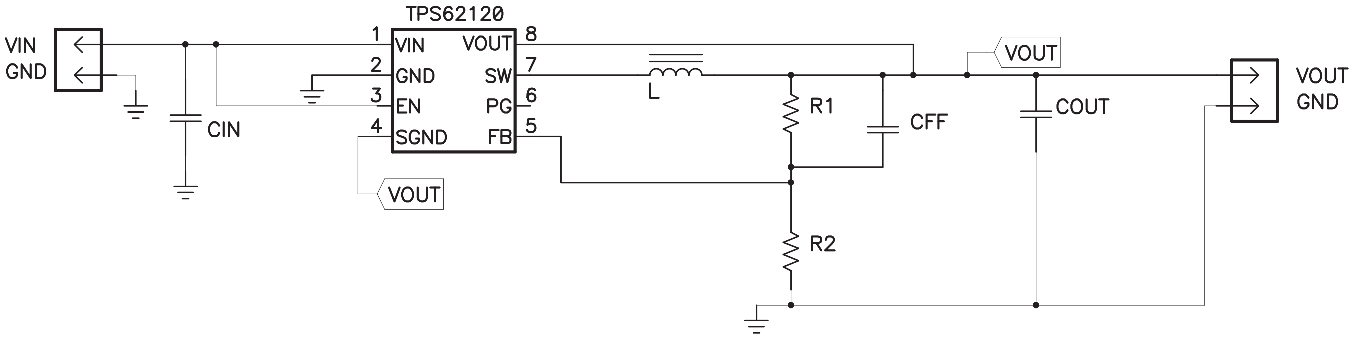


Figure 1. TPS62120 Buck Topology

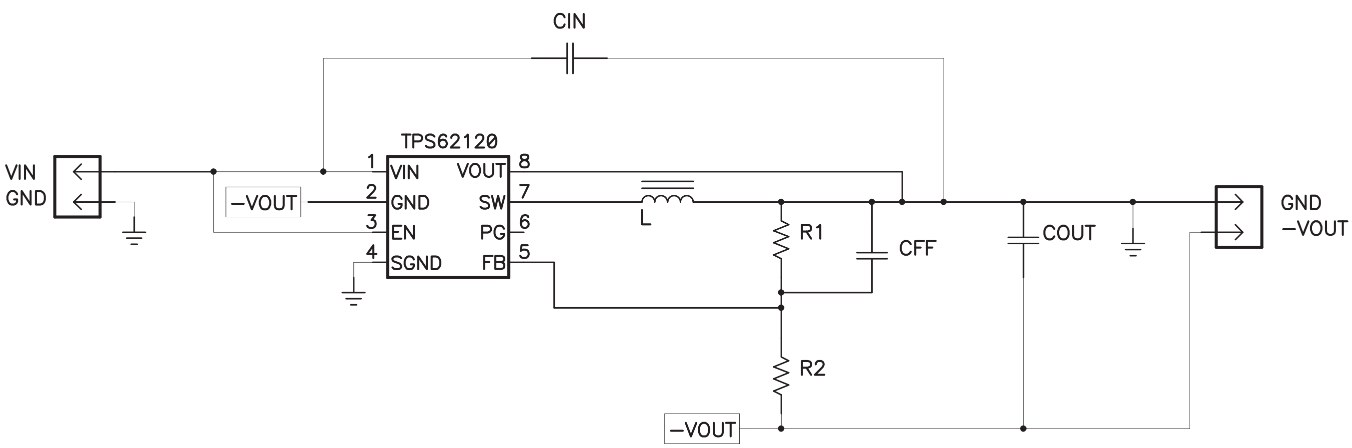


Figure 2. TPS62120 Inverting Buck-Boost Topology

The circuit operation is different in the inverting buck boost topology than in the buck topology. Figure 3 **(a)** illustrates that the output voltage terminals are reversed, though the components are wired the same as a buck converter. During the on time of the control MOSFET, shown in Figure 3 **(b)**, the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the off time of the control MOSFET and the on time of the synchronous MOSFET, shown in Figure 3 **(c)**, the inductor provides current to the load and the output capacitor. These changes affect many parameters described in the upcoming sections.

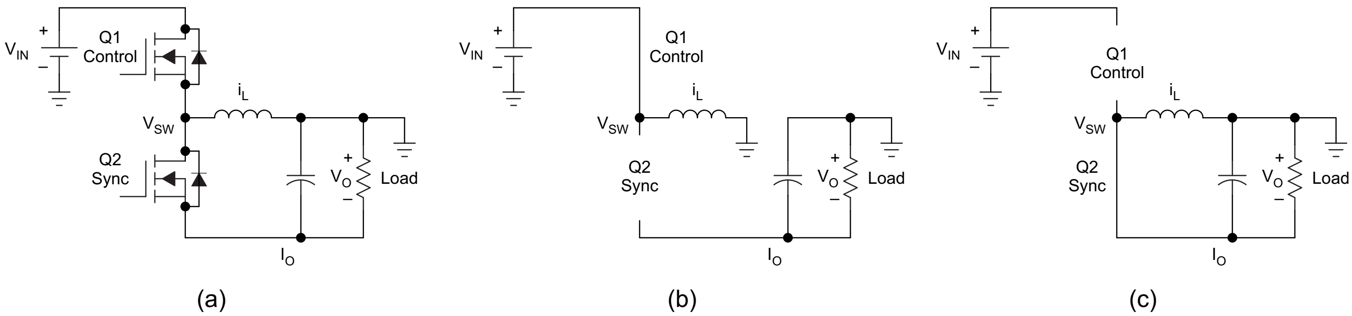


Figure 3. Inverting Buck-Boost Configuration

1.2 Output Current Calculations

The average inductor current is affected in this topology. In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on and off times of the control MOSFET. However, in the inverting buck boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on time of the control MOSFET. During the off time, the inductor connects to both the output cap and the load (see Figure 3). Knowing that the off time is 1 – D of the switching period, then the average inductor current is:

$$I_{L(Avg)} = \frac{I_{OUT}}{(1 - D)} \quad (1)$$

The duty cycle for the typical buck converter is simply V_{OUT} / V_{IN} but the duty cycle for an inverting buck boost converter becomes:

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN})} \quad (2)$$

Finally, the maximum inductor current becomes:

$$I_{L(Max)} = I_{L(Avg)} + \frac{\Delta I_{L(Max)}}{2} \quad (3)$$

Where,

D: Duty cycle

ΔI_L (A): Peak to peak inductor ripple current

V_{IN} (V): Input voltage with respect to ground, instead of IC ground or $-V_{OUT}$.

The TPS62120's current limit technique allows a simple maximum output current calculation. If the current exceeds I_{LIMF} (the high-side MOSFET current limit), the high-side MOSFET switch turns off and the low-side MOSFET switch turns on until the inductor current ramps down to 0. If an overload is still present after reaching 0 current, the low-side MOSFET switch turns off and the high-side MOSFET switch turns on until current limit is reached again. In current limit, the inductor's current goes from I_{LIMF} to 0—its ripple current becomes I_{LIMF}. Operating the TPS62120 in this state (with $I_{L(Max)}$ equal to $\Delta I_{L(Max)}$ equal to I_{LIMF}) reduces the average inductor current to ½ I_{LIMF} (from Equation 3). With the TPS62120's minimum current limit value of 200 mA, this gives an $I_{L(Avg)}$ of 100 mA when current limit is reached. With this, the maximum allowable output current is calculated from Equation 1 and Equation 2, with a 5-V input voltage to –5-V output voltage system as an example:

D = –5 / (–5 – 5) = 0.5

This result is then used in Equation 1:

$I_{OUT} = I_{L(Avg)} \times (1 - D) = 100 \times (1 - 0.5) = 50$ mA

The maximum output current for –5 V, –3.3 V and –1.8 V output voltages at different input voltages is displayed in Figure 4.

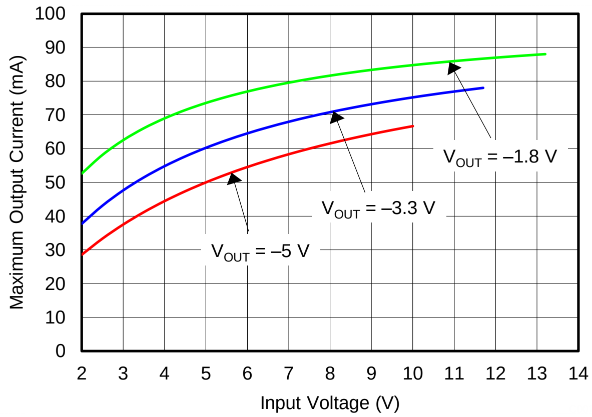


Figure 4. Maximum Output Current versus Input Voltage

1.3 V_{IN} and V_{OUT} Range

The input voltage that can be applied to an inverting buck boost converter IC is less than the input voltage that can be applied to the same buck converter IC. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, not V_{IN} to ground. Thus, the input voltage range of the TPS62120 is 2 V to 15 + V_{OUT}, where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but negative. The output voltage for the inverting buck boost topology should be set between –1.2 V and –5.5 V. It is set the same way as in the buck configuration, with two resistors connected to the FB pin.

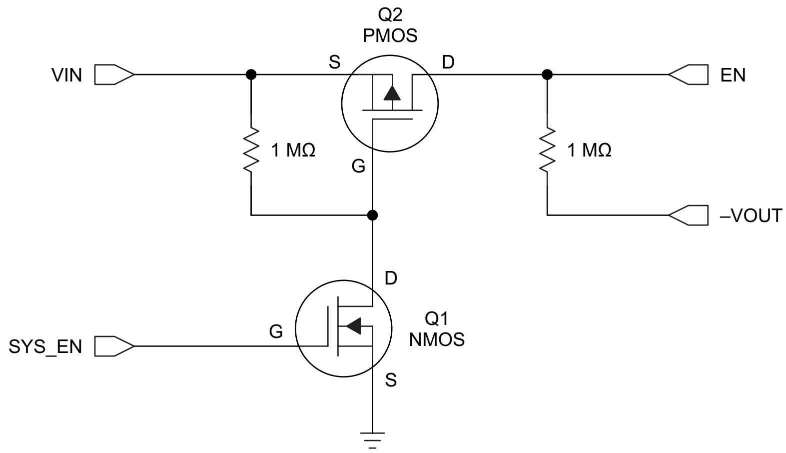
2 Digital Pin Configurations

2.1 Enable Pin

The device is enabled once the voltage at the EN pin trips its threshold and the input voltage is above the UVLO threshold. The TPS62120 stops operation once the voltage on the EN pin falls below its threshold or the input voltage falls below the UVLO threshold.

Because V_{OUT} is the IC ground in this configuration, the EN pin must be referenced to V_{OUT} instead of ground. In the buck configuration, 1.1 V is considered a high and less than 0.4 V is considered a low. In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 1.1 V + V_{OUT} and the low threshold is 0.4 V + V_{OUT}. For example, if V_{OUT} = –5 V, then V_{EN} is considered at a high level for voltages above -3.9 V and a low level for voltages below –4.6 V.

This behavior can cause difficulties enabling or disabling the part, since in some applications, the IC providing the EN signal may not be able to produce negative voltages. The level shifter circuit shown in Figure 5 alleviates any difficulties associated with the offset EN threshold voltages by eliminating the need for negative EN signals. If disabling the TPS62120 is not desired, the EN pin may be directly connected to V_{IN} without this circuit.



NOTE: VOUT is the negative output voltage of the inverting buck-boost converter

Figure 5. EN Pin Level Shifter

The positive signal that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN grounded), Q2 sees 0 V across its V_{GS}, and also remains off. In this state, the EN pin sees –5 V which is below the low-level threshold and it disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (V_{GS} threshold as specified in the MOSFET datasheet), the gate of Q2 sees ground through Q1. This drives the V_{GS} of Q2 negative and turns Q2 on. Now, V_{IN} ties to EN through Q2 and the pin is above the high-level threshold, turning the device on. Be careful to ensure that the V_{GD} and V_{GS} of Q2 remain within the MOSFET ratings during both the enabled and disabled states. Failing to adhere to this constraint can result in damaged MOSFETs.

The enable and disable sequence is illustrated in Figure 6 and Figure 7. The SYS_EN signal activates the enable circuit, and the GD Node signal represents the shared node between Q1 and Q2. This circuit was tested with a 1.8-V SYS_EN signal and dual N/PFET Si1029X. The EN signal is the output of the circuit and goes from V_{IN} to $–V_{OUT}$ properly enabling and disabling the device. The SGND pin was used to accelerate V_{OUT}'s return to 0 V, when the IC is disabled.

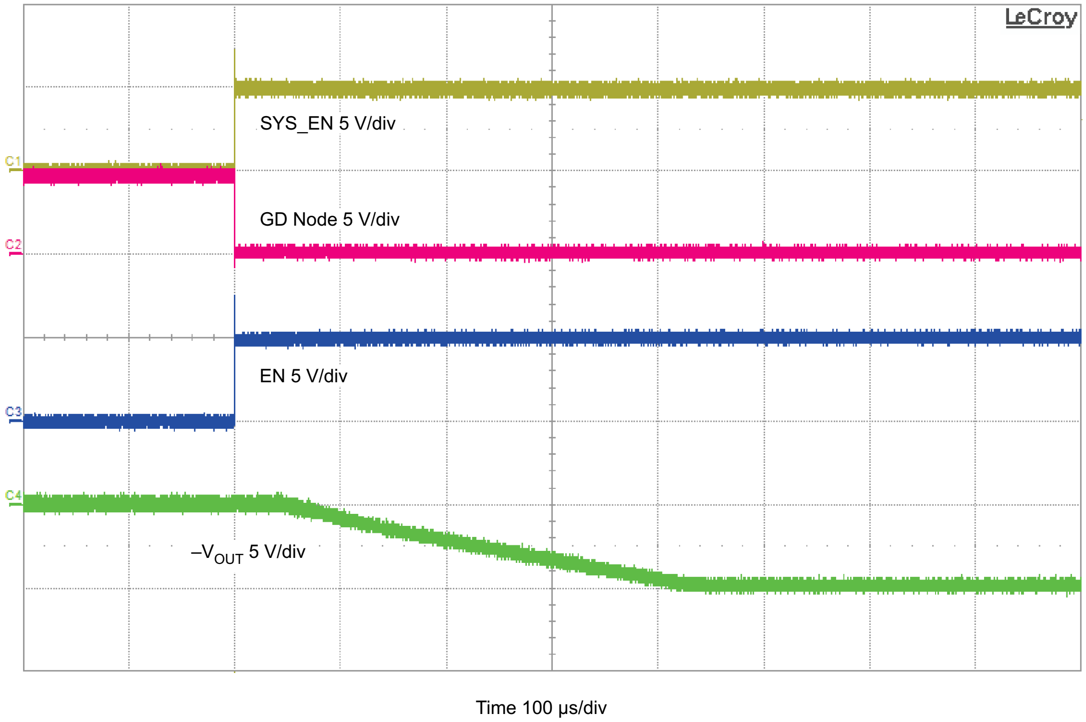


Figure 6. Enable Sequence

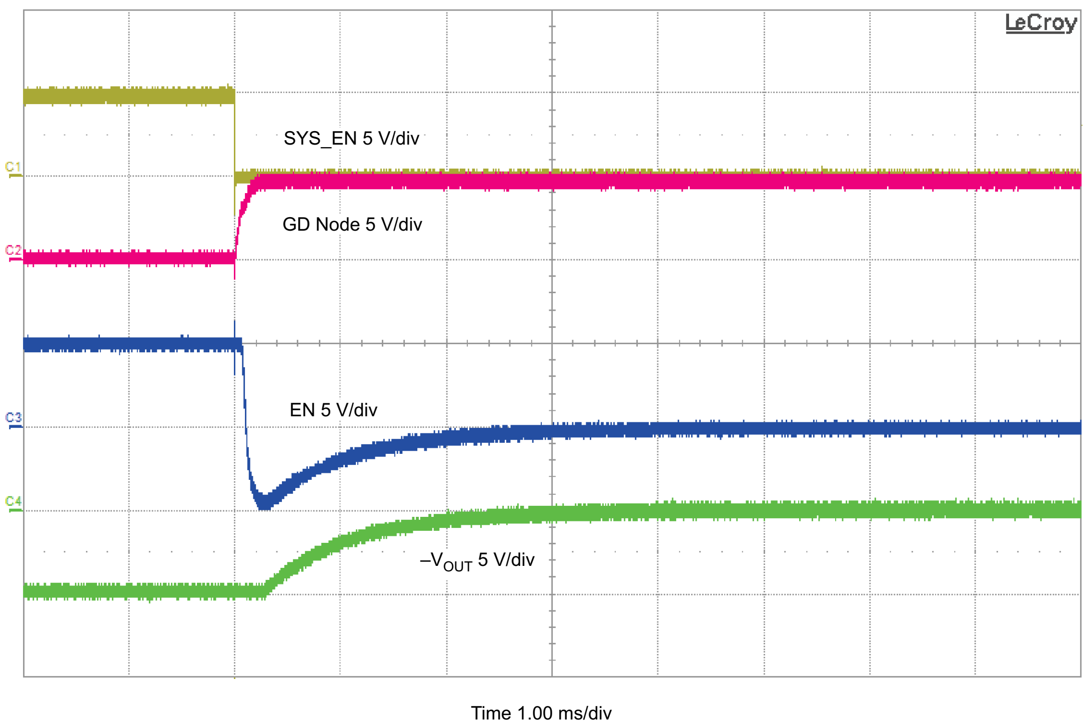


Figure 7. Disable Sequence

2.2 SGND Pin

SGND is an NMOS open-drain output pin that can be used to discharge the output capacitor. The internal NMOS connects the SGND pin to the IC ground (which is V_{OUT}) once the device is shutdown. It becomes high impedance once the device is enabled. The SGND pin should be connected to ground to operate this discharge function in the same way as a buck converter. If not used, SGND may be left floating or connected to V_{OUT}. Figure 8 shows the SGND internal circuit.

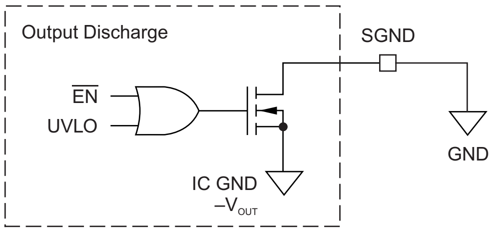


Figure 8. SGND Internal Circuit

2.3 Power Good Pin

The TPS62120 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because V_{OUT} is the IC ground in this configuration, the PG pin is referenced to V_{OUT} instead of ground, which means that the TPS62120 pulls PG to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin may not be able to withstand negative voltages. The level shifter circuit shown in Figure 9 alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it may be left floating or connected to V_{OUT} without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin should not be driven more than 6 V above the negative output voltage (IC ground).

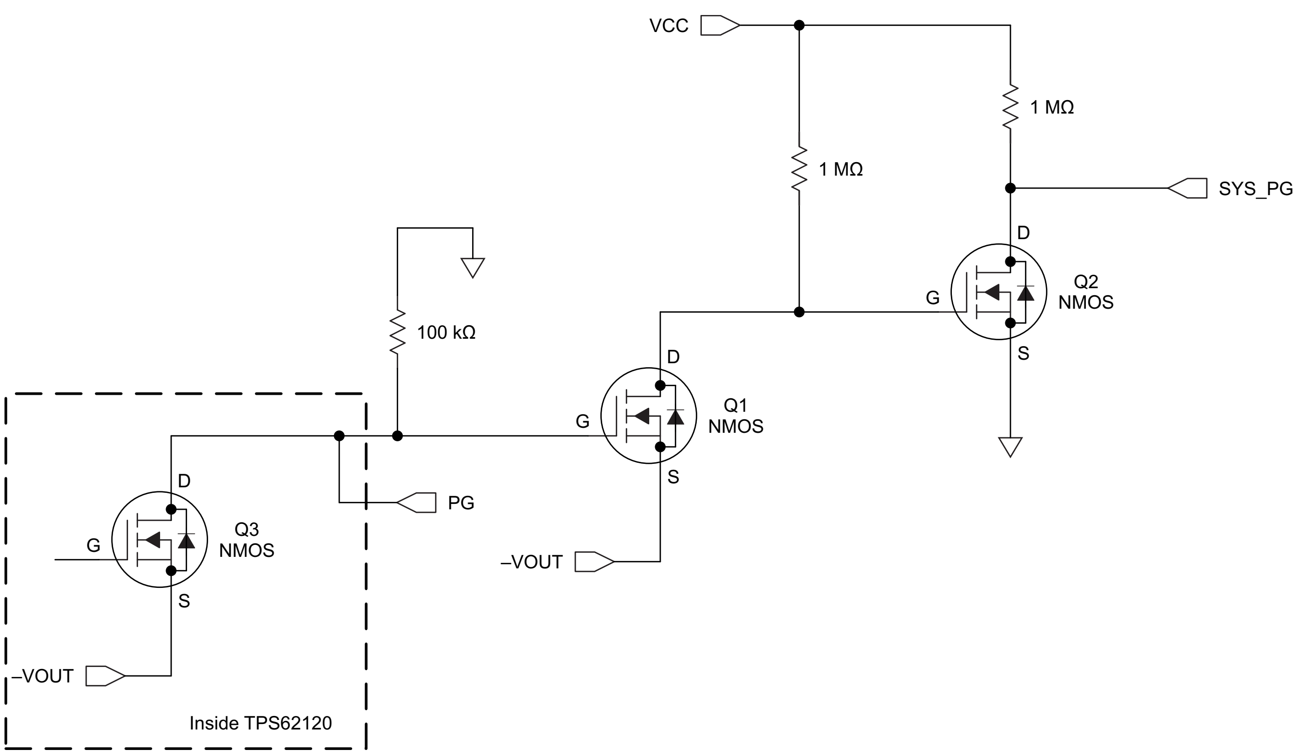


Figure 9. PG Pin Level Shifter

Inside the TPS62120, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is off and Q2 is on because its V_{GS} sees V_{CC}. SYS_PG is then pulled to ground.

When Q3 turns off, the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PG is then pulled up to the V_{CC} voltage. Note that the V_{CC} voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG net.

This PG pin level shifter sequence is illustrated in Figure 10 and Figure 11. The PG signal activates the PG pin level shifter circuit, and the GD Node signal represents the shared node between Q1 and Q2. This circuit was tested with a V_{CC} of 1.8 V and dual NFET Si1902DL. The SYS_PG net is the output of the circuit and goes between ground and 1.8 V, and is easily read by a separate device. The SGND pin was used to accelerate V_{OUT}'s return to 0 V, when the IC is disabled.

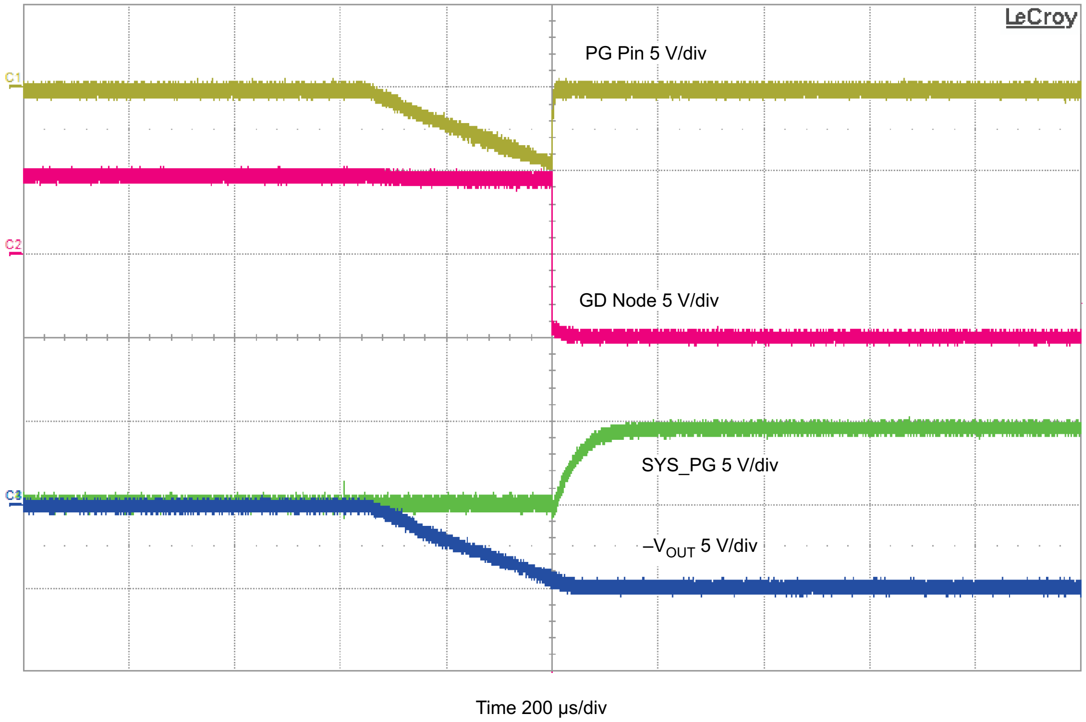


Figure 10. PG Pin Level Shifter on Startup

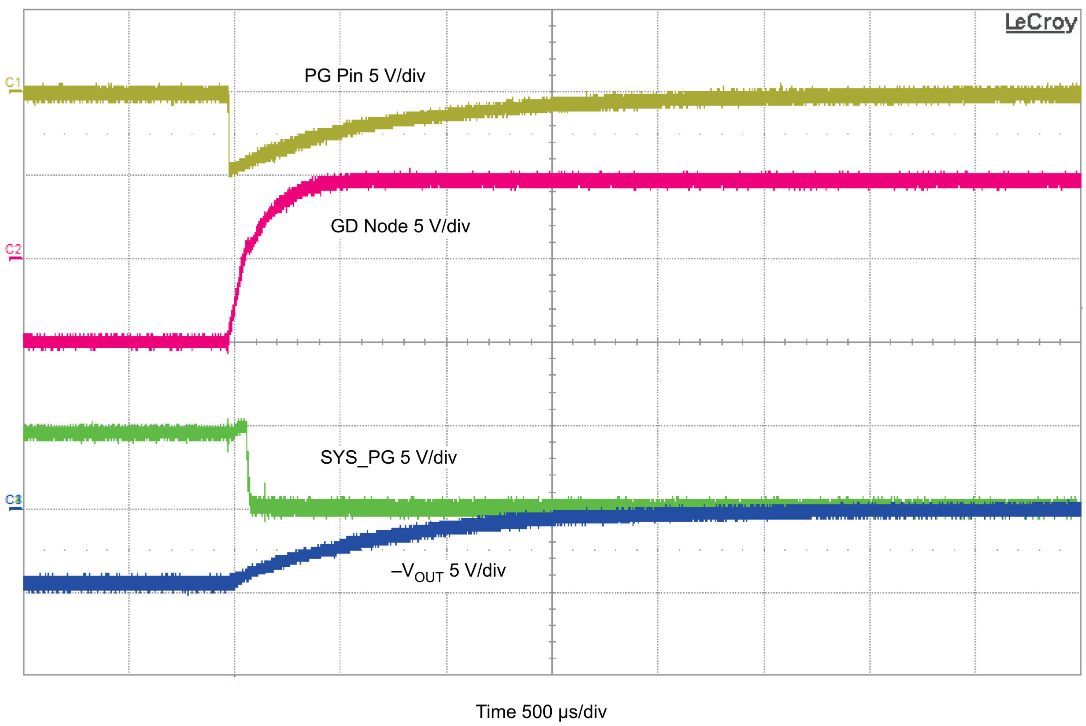


Figure 11. PG Pin Level Shifter on Shutdown

3 Startup Behavior and Switching Node Consideration

Figure 12 shows the startup behavior in the inverting configuration. After EN is taken high, the device starts switching after about a 50-µs delay. Due to the higher peak currents in the inverting topology, current limit is frequently reached during startup. This is acceptable as long as the saturation current of the inductor is chosen appropriately.

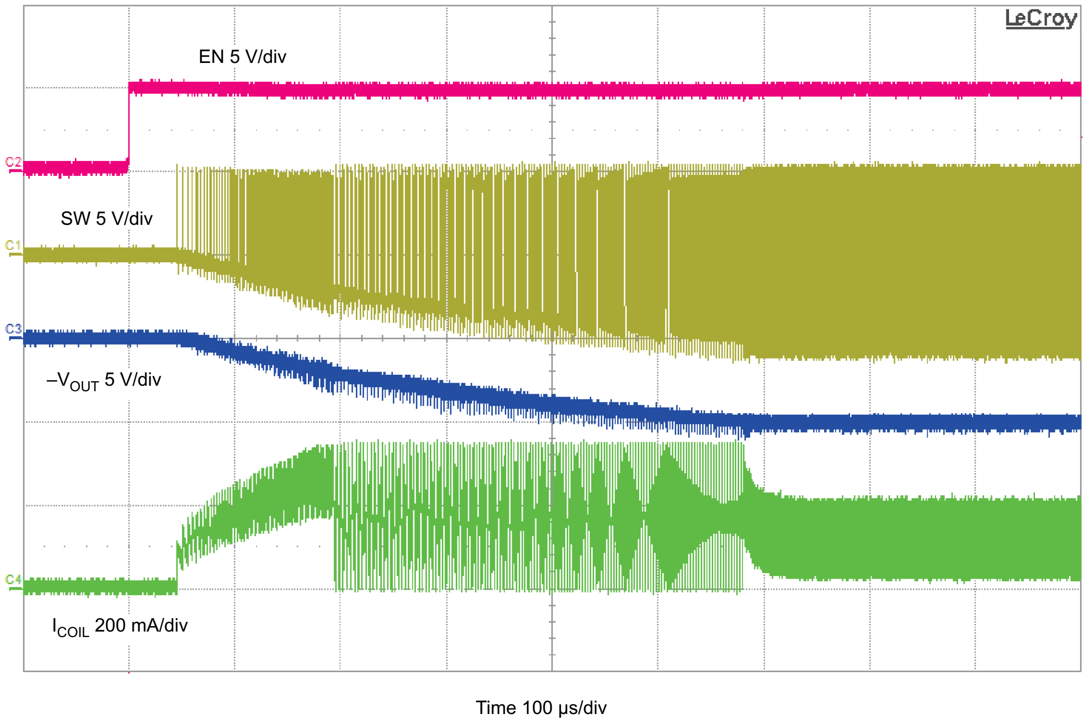


Figure 12. Startup Behavior in the Inverting Configuration

Figure 12 also shows the SW node voltage as the device starts up. The voltage on the SW pin switches from V_{IN} to V_{OUT}. As the high-side MOSFET turns on, the SW node sees the input voltage and as the low-side MOSFET turns on, the SW node sees the IC ground, which is the output voltage. As V_{OUT} continues to ramp down, the SW node low level follows it down.

4 External Component Selection

The inductor and output capacitor need to be selected based on the needs of the application and the stability criteria of the device. The selection criterion for the inductor and output capacitor is different from the buck converter. See Section 4.3 for a discussion of stability.

4.1 Inductor Selection

When selecting the inductor value for the inverting buck boost topology, the equations provided in Output Current Calculations should be used instead of the ones provided in the data sheet. ($I_{L(max)}$ should be kept below the minimum current limit value of the device (0.2 A) for a reliable design.) It is recommended to size the inductor for the current limit level of the TPS62120, as this level is sometimes reached during startup (shown in Figure 12). See Section 4.3 for the stability impact of the inductor selection.

4.2 Input Capacitor Selection

An input capacitor, C_{IN}, is required to provide a local bypass for the input voltage source. A low ESR input capacitor is best for input voltage filtering and minimizing interference with other circuits. For most applications, a 10-µF ceramic capacitor is recommended from V_{IN} to ground (system ground, not $-V_{OUT}$). The C_{IN} capacitor value can be increased without any limit for better input voltage filtering.

For the inverting buck boost configuration of the TPS62120, it is not recommended to install a capacitor from V_{IN} to $–V_{OUT}$. Such a capacitor, if installed, provides an AC path from V_{IN} to $–V_{OUT}$. When V_{IN} is applied to the circuit, this dV/dt across a capacitor from V_{IN} to $–V_{OUT}$ creates a current that must return to ground (the return of the input supply) to complete its loop. This current might flow through the internal low-side MOSFET's body diode and the inductor to return to ground. Flowing through the body diode pulls the SW pin and VOS pin more than 0.3 V below IC ground, violating their absolute maximum rating. Such a condition might damage the TPS62120 and is not recommended. Therefore, a capacitor from V_{IN} to $–V_{OUT}$ is not needed or recommended. If such a capacitor (CBP) is present, then a Schottky diode should be installed on the output, per Figure 13. Startup testing should be conducted to ensure that the VOS pin is not driven more than 0.3 V below IC ground when V_{IN} is applied.

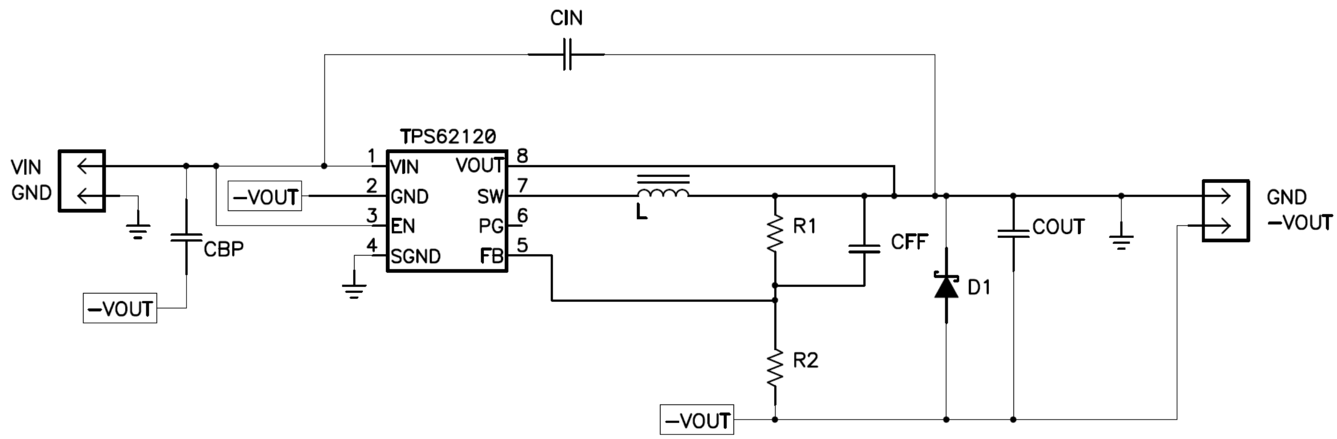


Figure 13. If Installing CBP, Installing Schottky D1 is Required

4.3 Selecting L and C_{OUT} for Stability

The switch node, inductor current, and the output voltage ripple during steady state are signals that need to be checked first for the stability of the system. Oscillations on the output voltage and the inductor current, and jitter on the switch node are good indicators of the instability of the system. Figure 21 shows both the switch node and output voltage ripple of this topology. Load transient response is another good test for stability, as described in the SLVA381 application report.

The recommended nominal inductor and output capacitor values to use for this topology are in the range of 18 µH to 22 µH and from 10 µF to 47 µF, respectively. In this application report, a 18-µH inductor and a 10-µF capacitor are used.

The inverting buck boost topology contains a Right Half Plane (RHP) zero which significantly and negatively impacts the control loop response by adding an increase in gain along with a decrease in phase at a high frequency. This can cause instability. Equation 4 estimates the frequency of the RHP zero.

$$f_{(RHP)} = \frac{-(1-D)^2 \times V_{OUT}}{(D \times L \times I_{OUT} \times 2 \times \pi)} \tag{4}$$

It is recommended to keep the loop crossover frequency to 1/10th of the RHP zero frequency. Doing this requires either decreasing the inductance to increase the RHP zero frequency or increasing the output capacitance to decrease the crossover frequency. Note that the RHP zero frequency occurs at lower frequencies with lower input voltages, which have a higher duty cycle. SLVA465 explains how to measure the control loop of a DCS-Control™ device while Figure 14 shows the bode plot of Figure 15.

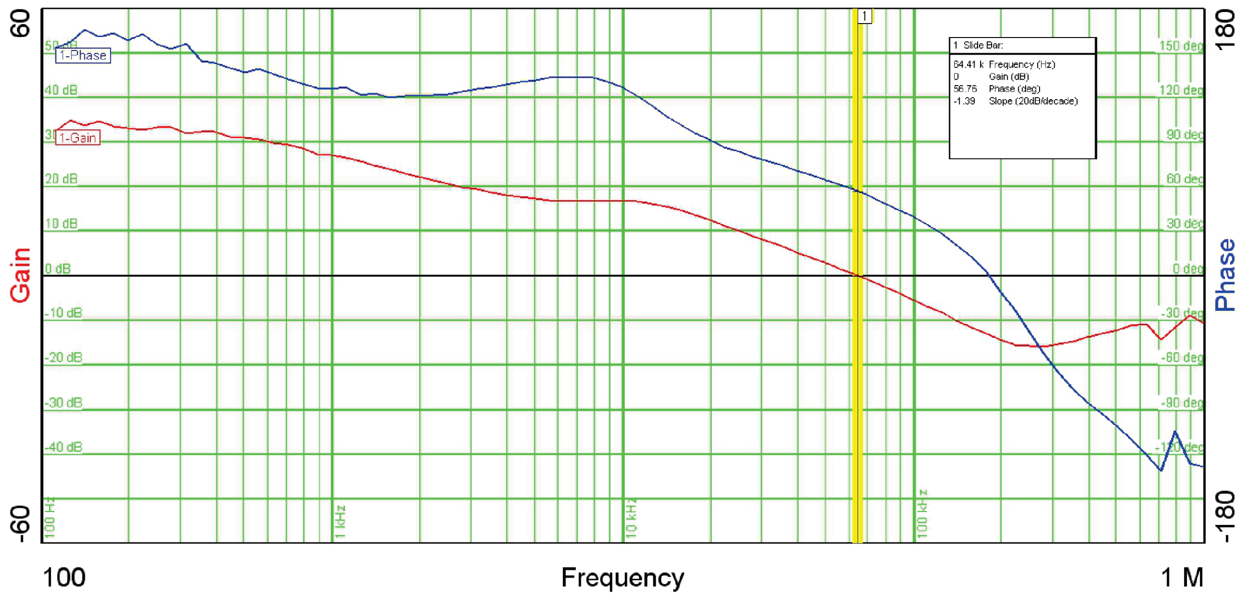


Figure 14. Bode Plot at 5-V V_{IN} and 50-mA Load

5 Typical Performance and Waveforms

The application circuit shown in Figure 15 is used to generate the data presented in Figure 16 – Figure 21. The output capacitor used is a 10-µF, 6.3-V, 0603, X5R ceramic capacitor. For a 5-V output, loss of capacitance from the DC bias effect can be significant. Unless otherwise specified, V_{IN} = 5 V and V_{OUT} = –5 V.

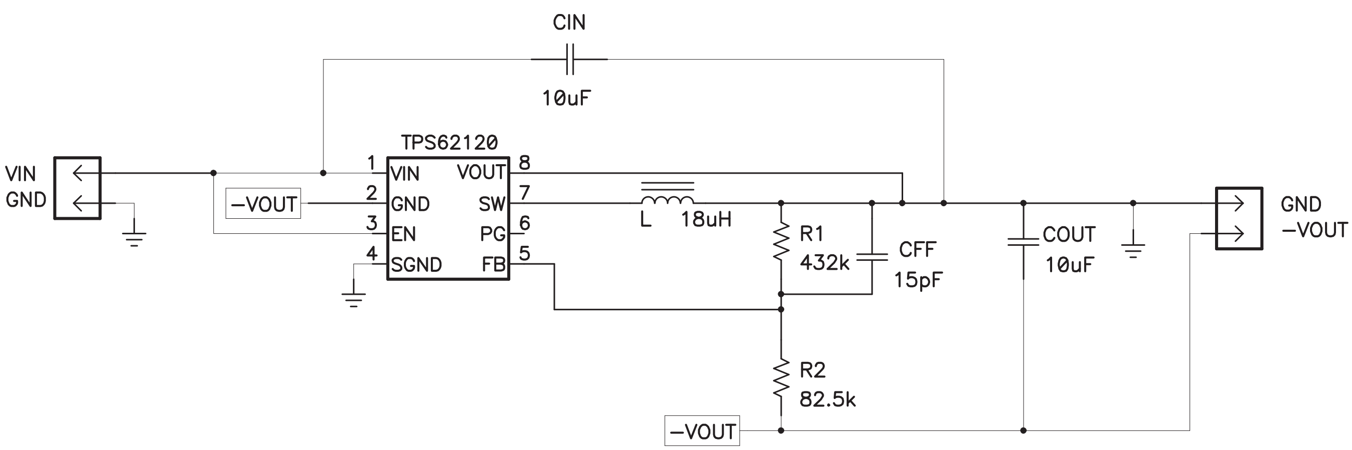


Figure 15. Schematic of the Tested Circuit

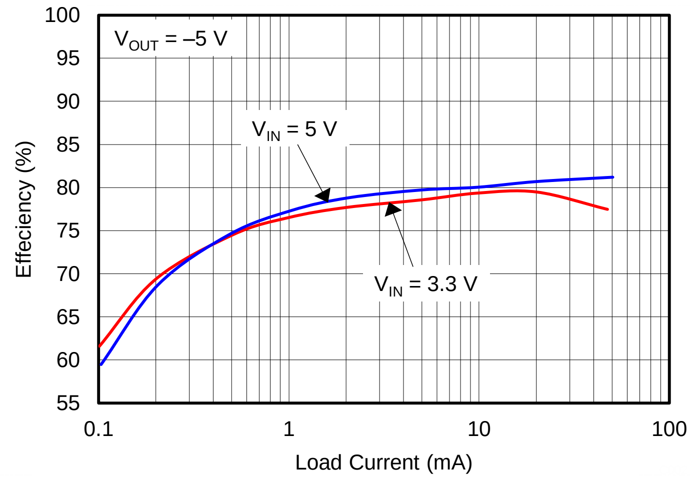


Figure 16. Efficiency versus Load Current with V_{OUT} = –5 V

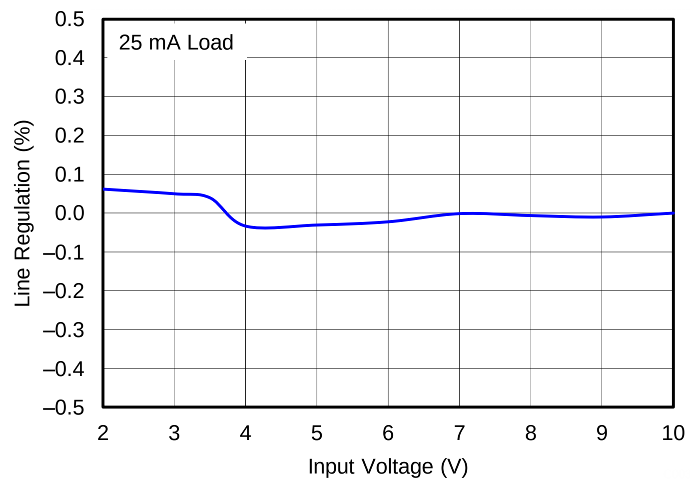


Figure 17. Line Regulation with V_{OUT} = –5 V and 25-mA Load

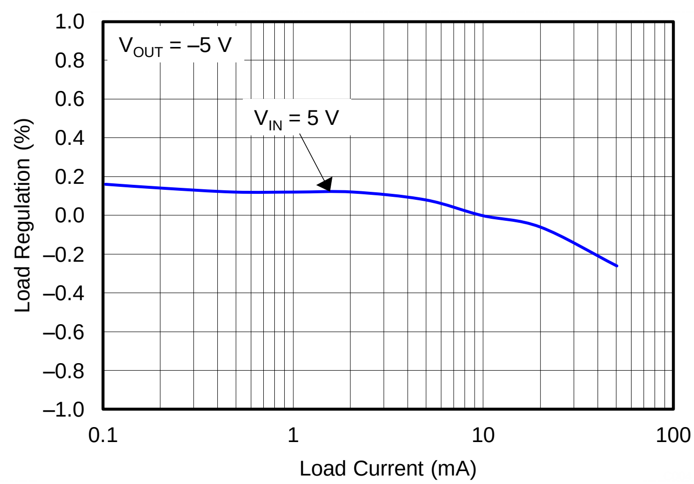


Figure 18. Load Regulation with V_{OUT} = –5 V

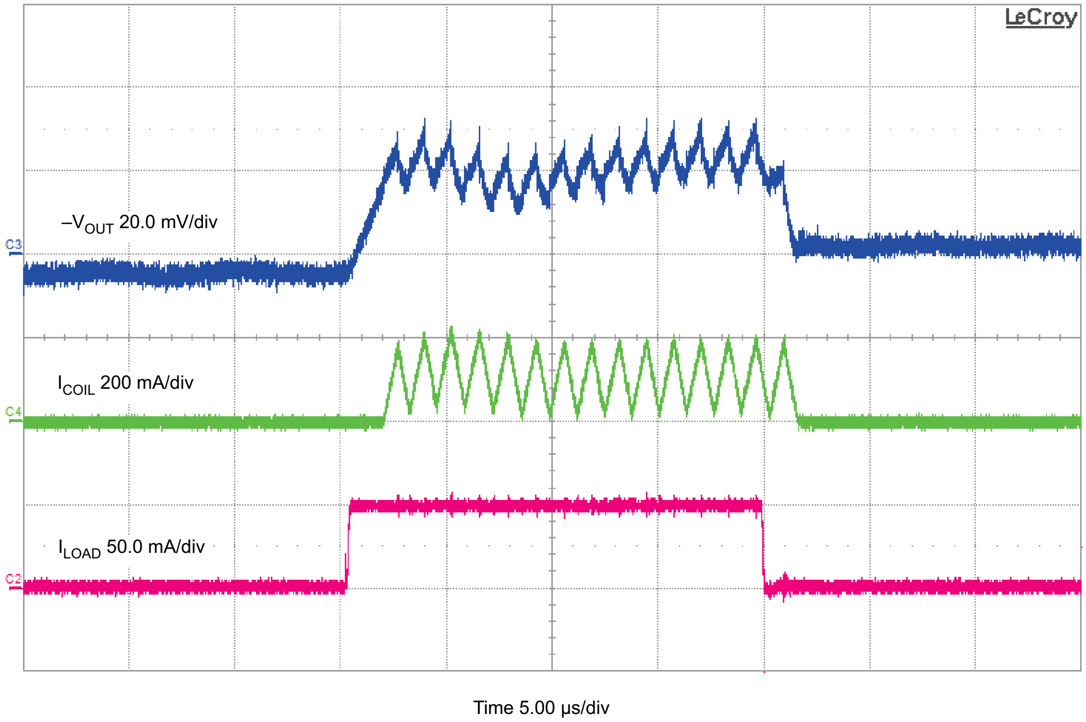


Figure 19. Load Transient Response 0 mA to 50 mA with V_{IN} = 5 V

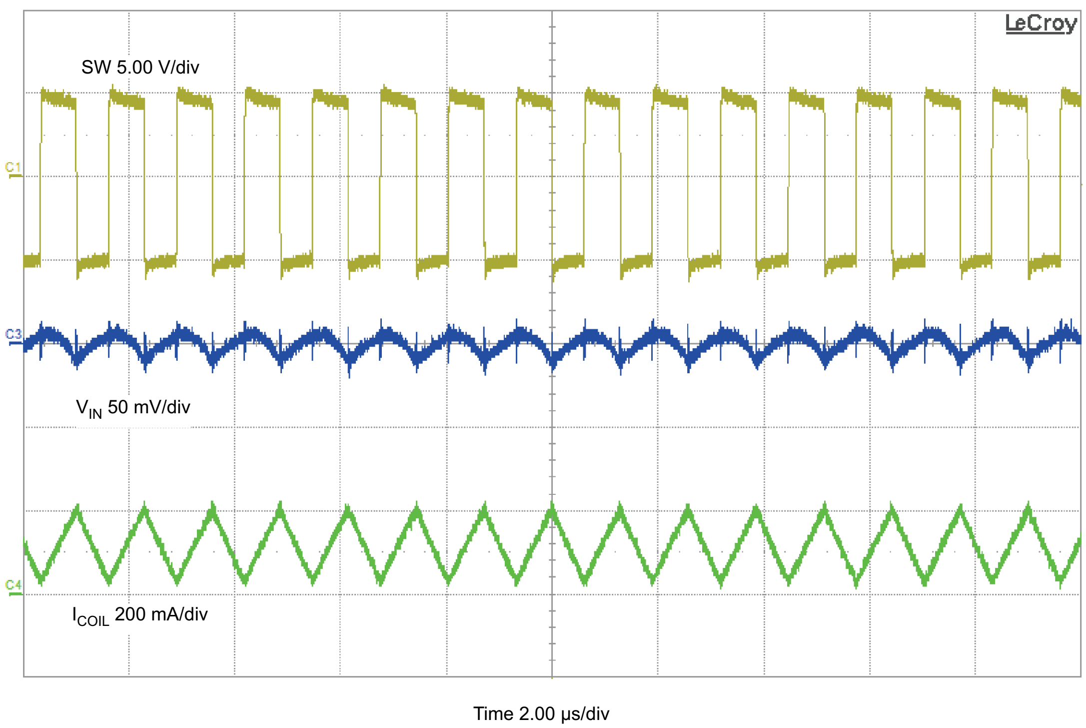


Figure 20. Input Voltage Ripple, V_{IN} = 5 V and I_{OUT} = 50 mA

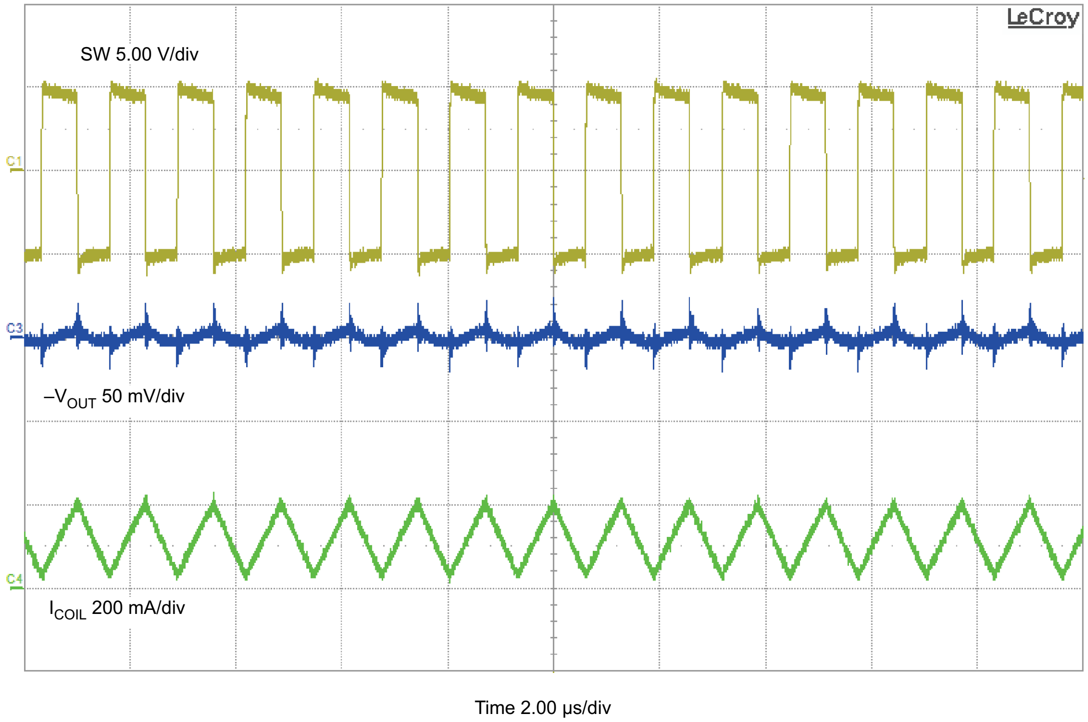


Figure 21. Output Voltage Ripple, V_{IN} = 5 V and I_{OUT} = 50 mA

6 Conclusion

The TPS62120 can be configured as an inverting buck-boost converter to generate a negative output voltage. The inverting buck-boost topology changes some system characteristics, such as input voltage range and maximum output current. This application report explains the inverting buck-boost topology and how to select the external components with the changed system characteristics. Measured data from the example design are provided. This report also applies to the TPS62122.

7 References

1. *Creating an Inverting Power Supply From a Step-Down Regulator* (SLVA317)
2. *TPS62120 Datasheet* (SLVSAG7)
3. *Using a Buck Converter in an Inverting Buck-Boost Topology* (SLYT286)
4. *Using the TPS5430 in an Inverting Buck-Boost Topology* (SLVA257)
5. *Using the TPS6215x in an Inverting Buck Boost Topology* (SLVA469)
6. *Simplifying Stability Checks* (SLVA381)
7. Robert W. Erickson: *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 1997
8. How to Measure the Control Loop of DCS-Control™ Devices (SLVA465)
9. DCS-Control™ Landing Page: www.ti.com/dcs-control