MAXWELL SERDES USB 3.0 PERSONALITY CARD

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REV	E3
VER	1.0

Designed for TI by Mistral Solutions Pvt Ltd

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	05th JUNE 2018	Drafted from Rev E2, Ver 1.0 schematics.	Mistral Design Team	AJIT MB	AJIT MB
0.2	05th JUNE 2018	Updated USB3 power switch.	Mistral Design Team	AJIT MB	AJIT MB
1.0	25th JULY 2018	Baselined	Mistral Design Team	AJIT MB	AJIT MB

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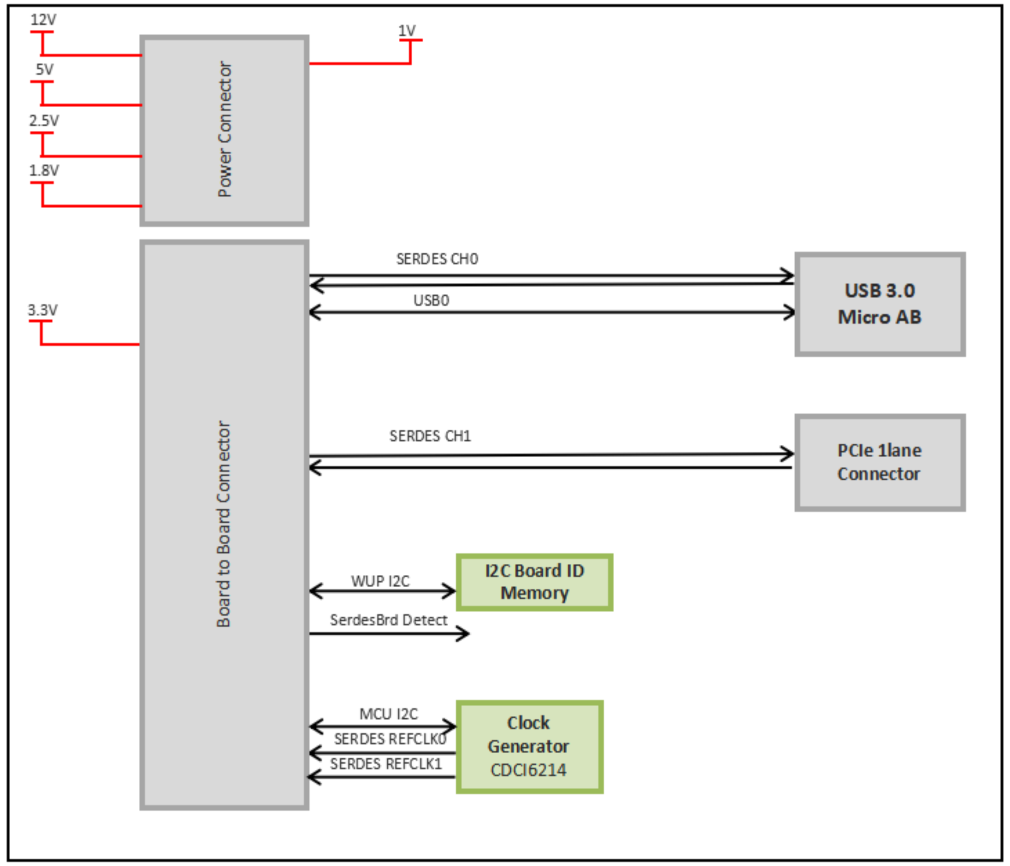
BLOCK DIAGRAM



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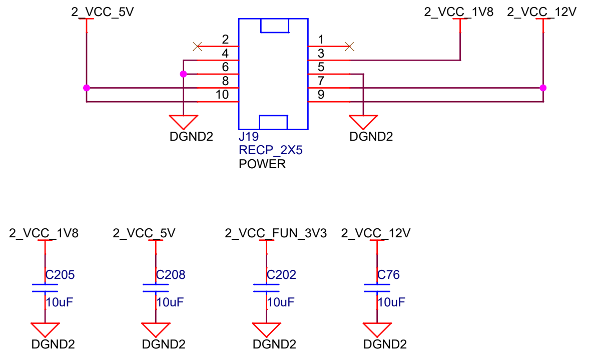
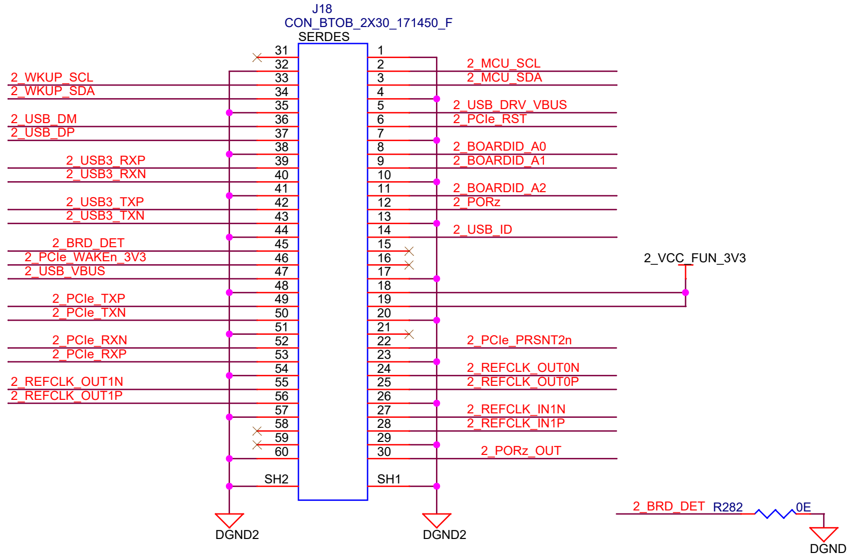
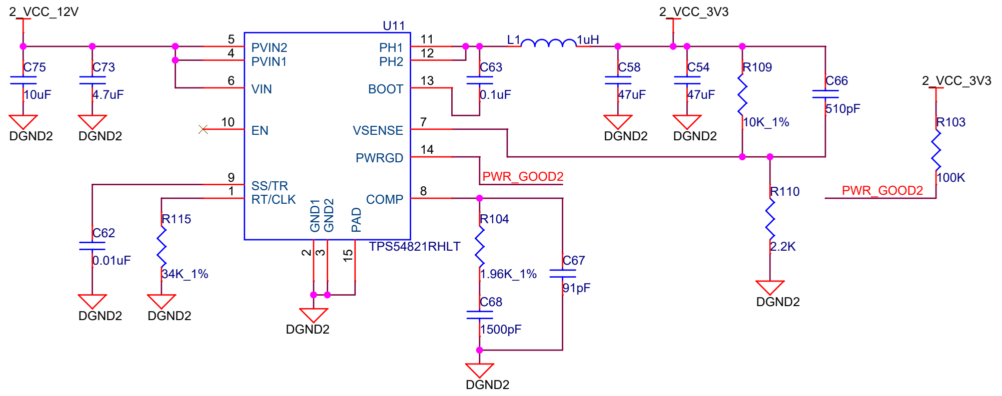
Power Connector



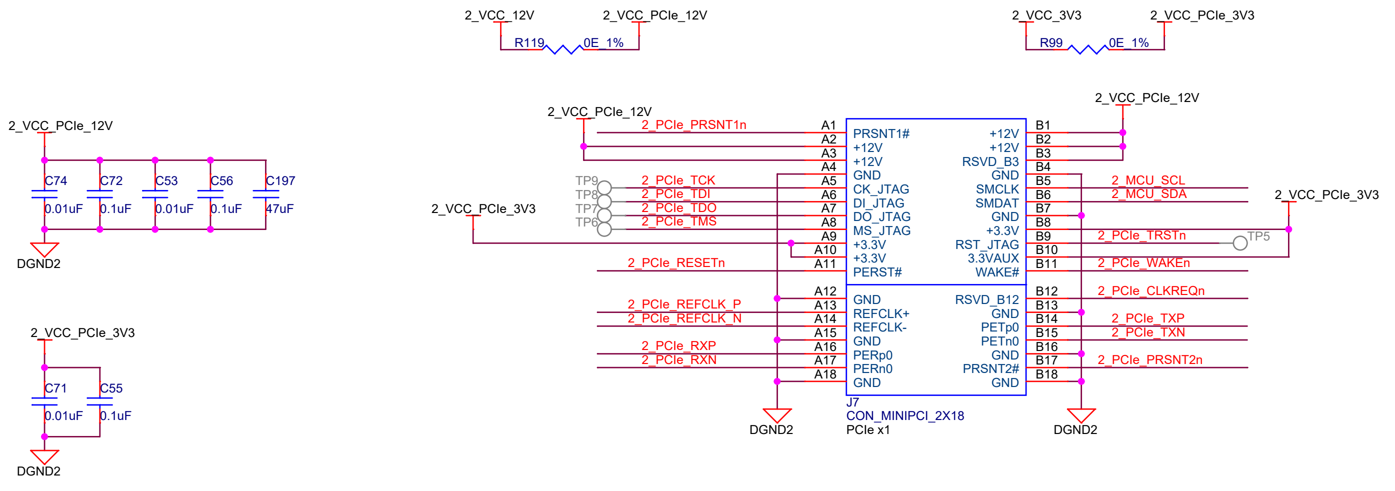
Serdes Connector



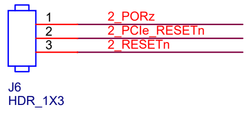
12V to 3.3V @ 6.5A Supply

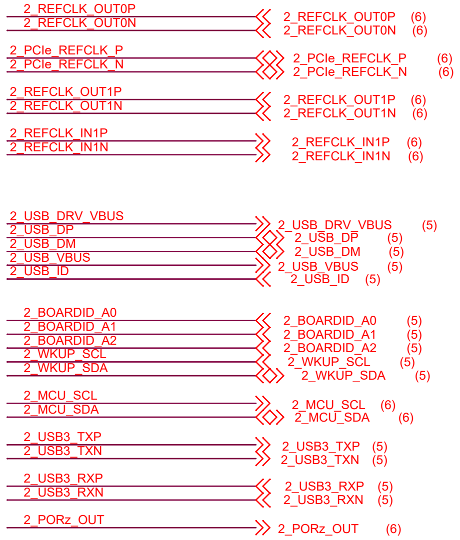


PCIe x1 Connectors

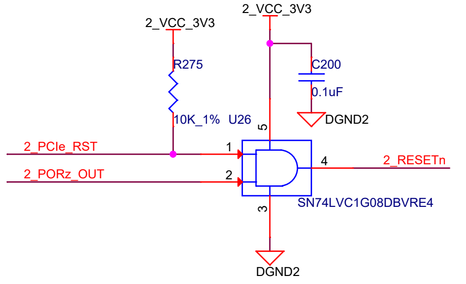


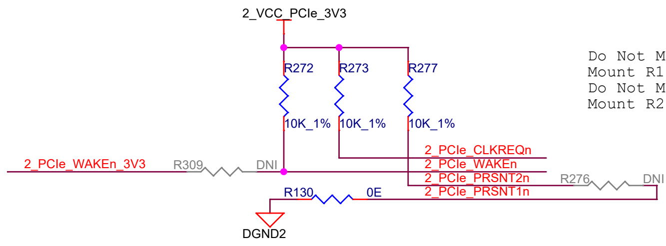
Short 1 and 2 for Device operation
Short 3 and 2 for Host operation





PCIe Reset





Do Not Mount R276 for Host operation
Mount R119, R99, R130 and R277 for Host operation
Do Not Maount 119, R99, R130 and R277 for Device operation
Mount R276 for Device operation

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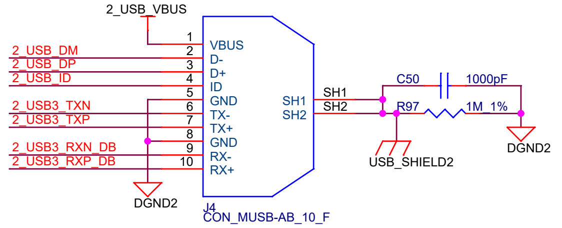
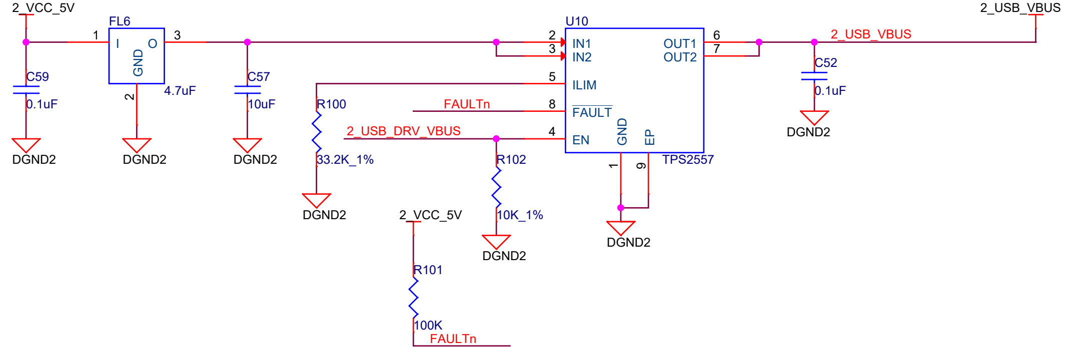
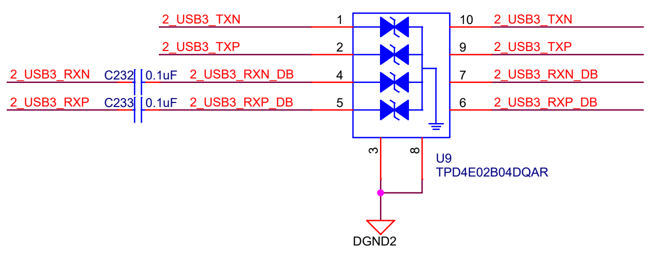
USB 3.0

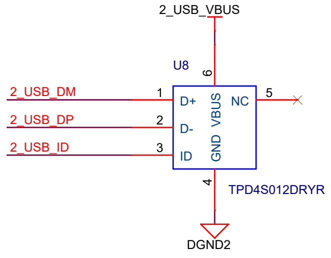
USB 3.0 micro AB Connector



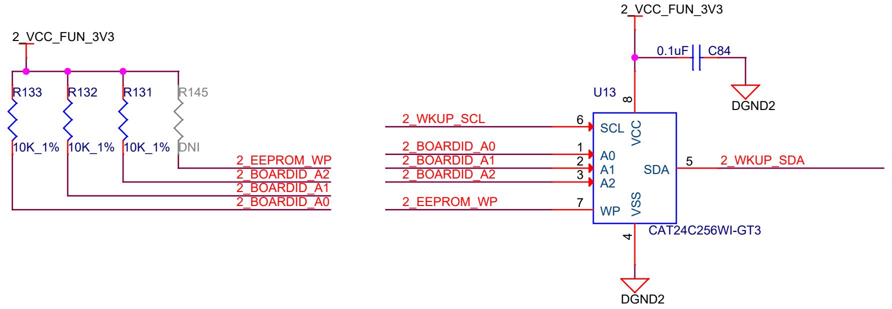
USB Power switch- 3A



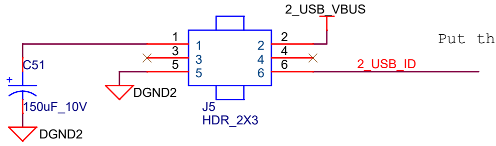




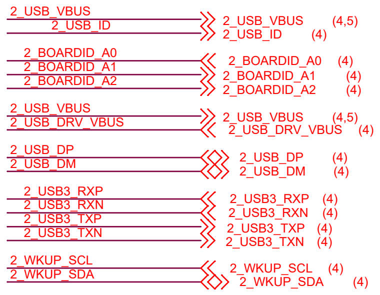
BOARD ID EEPROM



I2C address: 0x54h or Set by CP board



Put the jumper for Host operation



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Title
1LANEPCIe_CLK, USB3.0&BRDID

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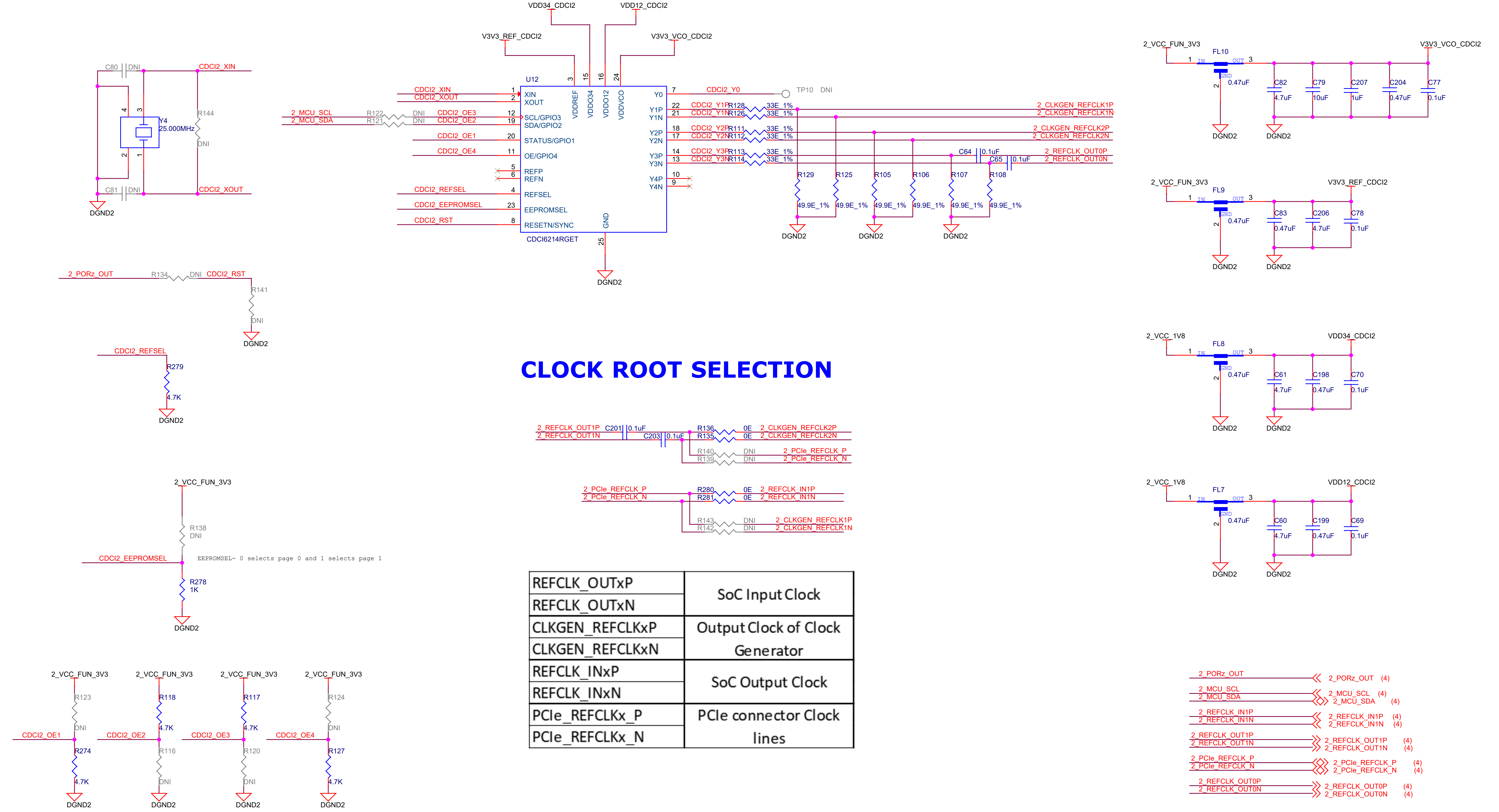
1LANE PCIe, USB3.0 Clock HCSL (100MHz) (EEPROM PAGE 0)



CLOCK ROOT SELECTION

REFCLK_OUTxP REFCLK_OUTxN	SoC Input Clock
CLKGEN_REFCLKxP CLKGEN_REFCLKxN	Output Clock of Clock Generator
REFCLK_INxP REFCLK_INxN	SoC Output Clock
PCIe_REFCLKx_P PCIe_REFCLKx_N	PCIe connector Clock lines

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TEXAS INSTRUMENTS

MISTRAL

Title
1LANEPCIe_CLK

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HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

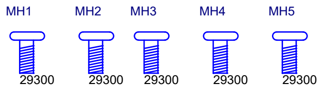
4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

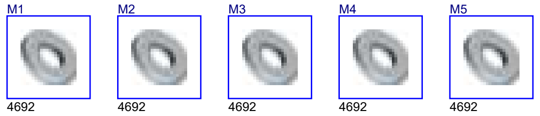
6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

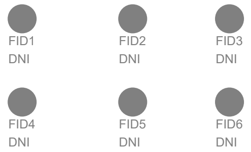
SCREWS



WASHER's



FIDUCIALS



LOGOs

PCB LOGO DNI	PCB LOGO DNI	PCB LOGO DNI	PCB LOGO DNI
Texas Intruments	**For Evaluation only; not FCC approved for resale**	**WEEE Mark**	**CE Mark**

BARE PCB

PCB1

PROC066

JUMPERs

ACC1

SPC02SYAN

`To be mounted on J14 pin 3 and 2 for Host operation.`

ACC2

MNT-103-BK-G

`To be mounted on J5 for USB Host operation.`

LABELS

Board Serial No.

LBL1

PCB LABEL

THT-103-423-10

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