Technical Article

Cycle Scavenging on C2000™ MCUs, Part 2: ADC Zero-wait-state and Multiport Reads

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As I explained in the first installment of this series, the idea of cycle scavenging is built into C2000™ microcontrollers (MCUs), enabling them to minimize latency at every stage of real-time control without compromising performance.

I introduced the concept of real-time control and talked about minimizing the time delay between the sensing, processing and actuation stages as one of the biggest challenges that engineers face in designing these systems. I also talked about C2000 microcontrollers being the right fit for these kinds of challenges due to the multitude of built-in cycle scavenging features that enable them to meet the strict timing demands of real-time control. In this installment, I'll focus on the sensing stage and take a look at two cycle-scavenging features: zero-wait-state analog-to-digital converter (ADC) transfers and ADC multiport reads.

C2000 MCUs prioritize the data paths from the ADC registers to the CPU, thus enabling zero-wait-state sample transfers out of the ADCs in a single CPU cycle. In other words, as soon as the ADC conversion is complete, the result can transfer immediately to the CPU without wasting any cycles.

Multiport ADC reads is another important feature unique to C2000 MCUs. In order to understand how multiport ADC reads fit into the theme of cycle scavenging, see the F28004x block diagram shown in Figure 1.

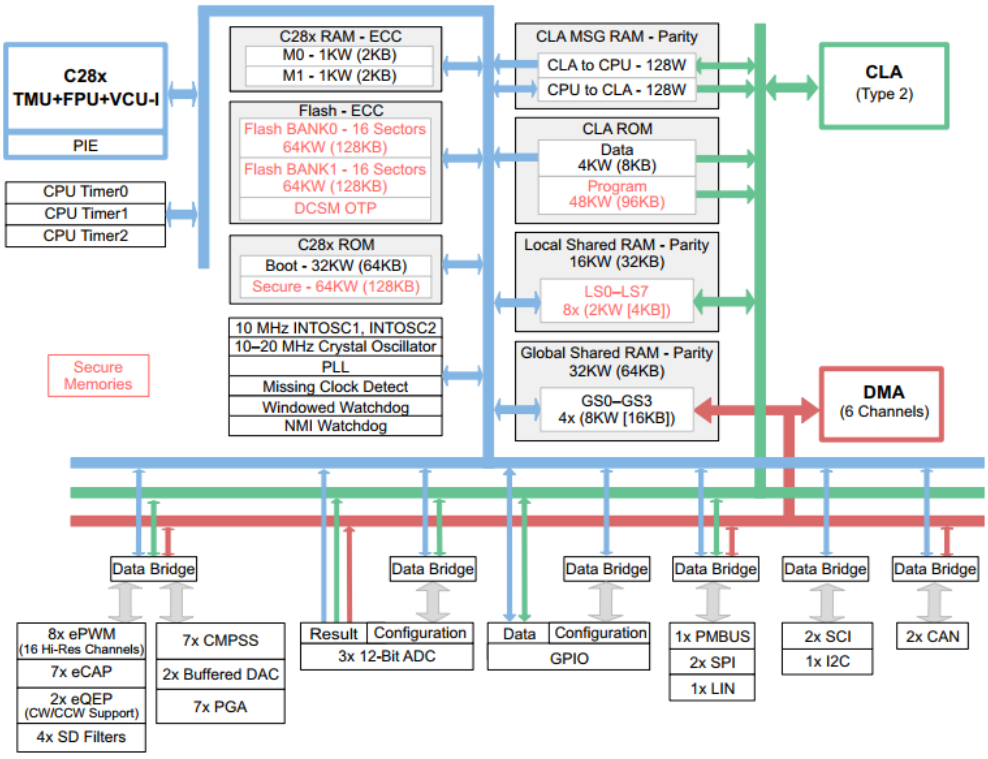

Figure 1. F28004x Block Diagram

Notice that while all peripherals have data bridges, the ADC result registers do not. This is very important from a cycle scavenging standpoint. The main purpose of a data bridge is to arbitrate between the masters

(central processing unit [CPU], control law accelerator [CLA] and direct memory access [DMA]). For example, if a situation arises where the DMA is moving words to/from the Serial Peripheral Interface (SPI) while the CPU tries to read the Local Interconnect Network (LIN) module in the same cycle, arbitration would occur because they share a data bridge. Such arbitration would result in one of the memory accesses being delayed by a cycle or so. If the ADC modules had a data bridge as well, there would be a delay every time multiple masters tried to access ADC results simultaneously. Such delays would adversely affect real-time control performance.

To avoid such delays in sensing, ADC registers have dedicated taps on each of the master buses, as shown in Figure 1. Thus, multiple masters can read the same or different results simultaneously as soon as they become available without any delay or arbitration, thereby saving cycles.

C2000 MCUs possess an array of features tuned to scavenge cycles at the sensing stage, but there's still more to come. In the next installment, I'll look at how ADC features like start-of-conversion timing and configurable ADC interrupt delays help with cycle scavenging.

Additional Resources:

- Keep up to date with our cycle scavenging blog series.
- Read our Fast Current Loop blog post, "Achieve unprecedented current-loop performance from an off-the-shelf MCU" and white paper, "A faster current loop pays off in servo motor control."
- Learn more about DesignDRIVE solutions for industrial servo and AC inverter drives.

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