TI Designs

4- to 20-mA Analog Input Module Reference Design for Safety Applications

Overview

The TIDA-00548 design is an isolated dual-channel 4- to 20-mA analog input reference design, which can be used as a sub-part for functional safety programmable logic controllers (PLCs). This reference design delivers digitized input values using a 32-bit high-performance analog-to-digital converter (ADC). The RM4x dual-core ARM® Cortex®-R4 based CPU with lockstep technology and built-in self-tests (BIST) compares the converted values of up to nine selectable analog input signal chain paths. The dual input approach with two separate burden resistors allows redundant measurement of either a single 4- to 20-mA loop or two independent loops. Hercules™ RM ARM Cortex-R based MCUs for functional safety applications (part of the SafeTI designs packages) help to develop systems according to IEC 61508 SIL 3.

Features

- Two-Channel, 4- to 20-mA Current Measurement for Redundancy
- Two ADC References (External and Internal)
- Small Burden Resistor (24.9 Ω)
- ADC Built-in Features, such as Test DAC, Secondary ADC, Analog Signal Level Alarm
- Isolator Shutdown Upon Failure Provides Reliable Notification to Back End
- All Integrated Circuits: MTBF Greater 4×10^8
- Designed in BeagleBone Cape Form Factor

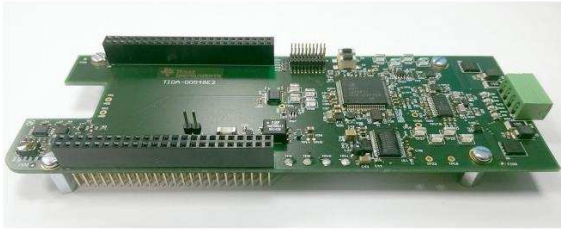
Applications

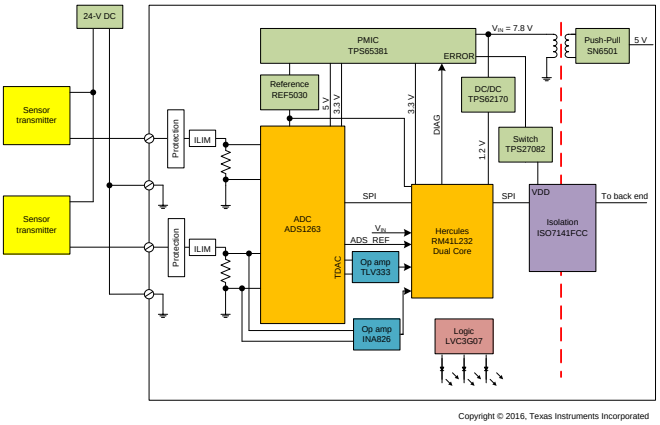
- Programmable Logic Controllers (PLCs)

Resources

TIDA-00548	Design Folder
RM41L232	Product Folder
ADS1263	Product Folder
TPS65381	Product Folder
REF5030	Product Folder
SN6501	Product Folder
TPS62170	Product Folder
TPS27082L	Product Folder
CSD18534Q5A	Product Folder
ISO7141CC	Product Folder
INA826	Product Folder
TLV333	Product Folder
BeagleBone Black Wiki	BeagleBone Resource Folder

TI E2E™ Community — ASK Our E2E Experts





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1 System Overview

1.1 System Description

The TIDA-00548 4- to 20-mA analog input module reference design assists in the development of safety analog input applications for PLCs. It is a subsystem of an analog input module covering the signal chain up to the isolation barrier towards the communication controller. The following items are primary components of this TI Design:

- SafeTI™ product Hercules dual-core look-step microcontroller (MCU)
- High-performance, 32-bit analog-to-digital converter (ADC)
- MCU companion power-management IC (PMIC)

The dual 4- to 20-mA analog input allows the connection of one or two sensor transmitters. A current limiter helps to the analog input and tolerates ±33 V because of wrong connections. EN61000-4-5 Class 2 (±1 kV at 24 A) surges at the input terminals can be handled. The analog input can take up to nine different signal paths to help ensure the correctness of the converted signal. The module is powered from the 5-V backplane power supply (BeagleBone Black) using isolated push-pull technology. Most of the required voltages are generated by a PMIC. The core voltage for the Hercules MCU is generated by a separate DC-DC converter. An external high-performance voltage reference is used to drive the external ADC and the ADC that is embedded in the Hercules MCU. The internal reference of the ADC is used as backup to compare against the external reference. Four LEDs visible at the terminal inputs allow fast status discovery of the board. The mean time between failure (MTBF) number of all TI components in this design is above 4×10^8 for robustness at the component level. The BeagleBone cape form factor plugs in easily on top of a BeagleBone (Black) board for rapid evaluation. The analog performance is better than compared to today's high-performance and high-resolution analog input modules available on the market. The full-scale error for such modules is in the range of ±0.1% at 25°C. This TI Design reaches a full-scale error of less than ±0.01% at room temperature during lab testing.

Figure 1 shows the physical board with a brief description of all connectors, buttons, jumpers, and LEDs.

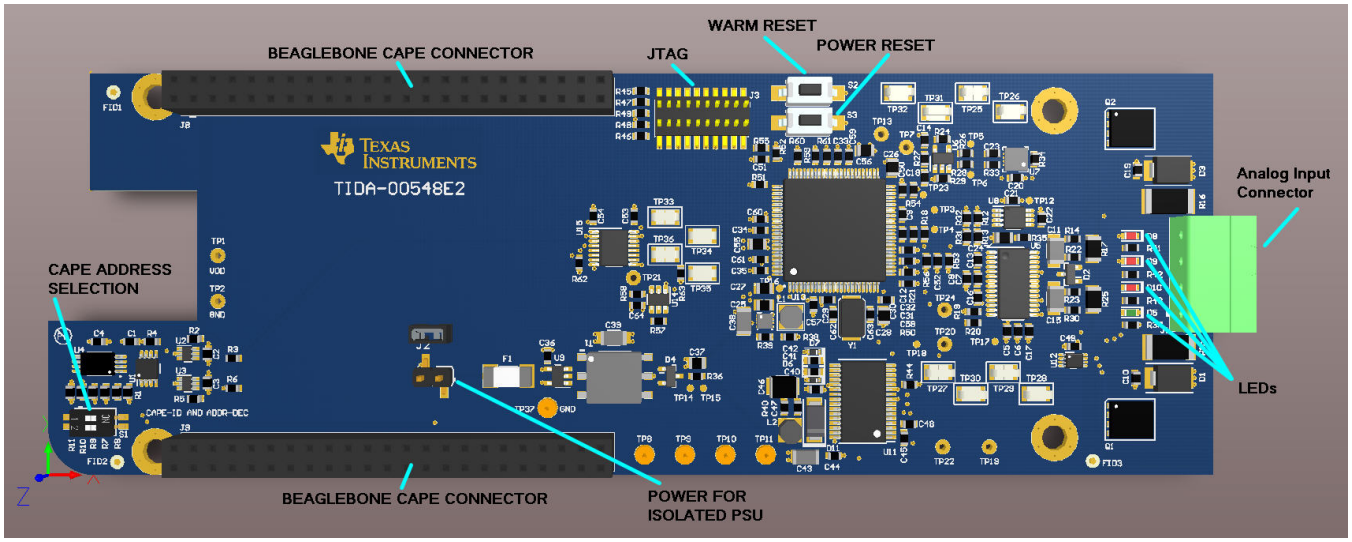

Figure 1. Physical Board

1.2 Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Number AI channels	2	Section 3.2
Operating voltage	4.3 to 5.25 V	Section 3.4
Power consumption	800 mW	Section 3.4
Analog input type	4- to 20-mA loop	—
Analog signal paths	9	Section 3.3
Input impedance	≈ 35 Ω	Section 3.2
Current limit	100 mA	Section 3.2
Full-scale error (offset cal 25°C)	±0.009%	Section 4.2
Effective bits	20	Section 4.1
Loop power supply	External	—
Signaling	Four LEDs at terminal inputs	Section 3.8
Surge transient immunity	EN 61000-4-5 class 2 (±1 kV, 24 A)	Section 3.2
Operating temperature	−40°C to 85°C	—
Form factor	159 × 55 mm (6.26 × 2.17 inch)	—

1.3 Block Diagram

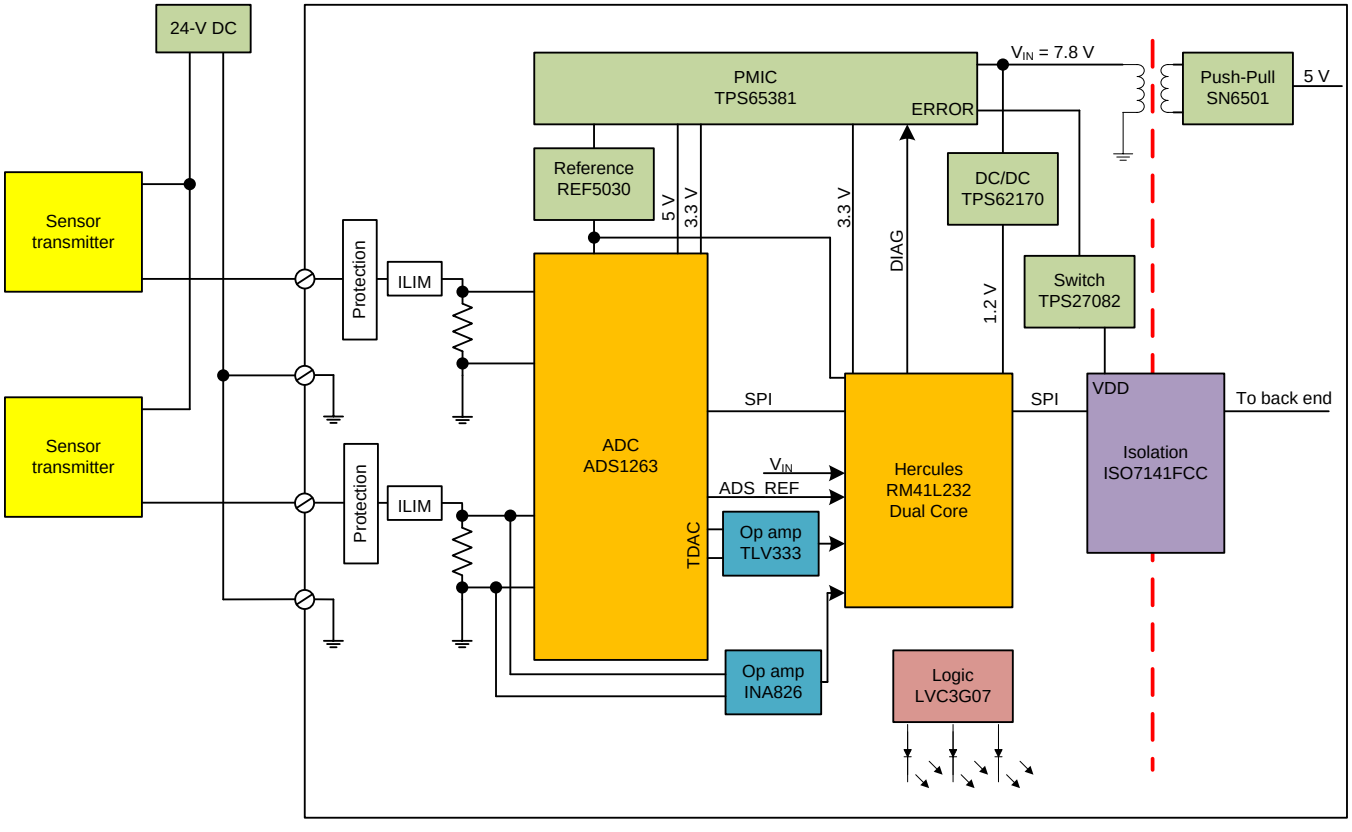

Figure 2. System Block Diagram

1.4 Highlighted Products

1.4.1 ADS1263

The ADS1263 is a low-noise, low-drift, 38.4-kSPS, delta-sigma (ΔΣ) ADCs with an integrated PGA, reference, and internal fault monitors. It integrates an auxiliary, 24-bit, ΔΣ ADC intended for background measurements. The sensor-ready ADCs provide complete, high-accuracy, one-chip measurement solutions for the most-demanding sensor applications, including weigh scales, strain-gauge sensors, thermocouples, and resistance temperature devices (RTD). The ADCs are comprised of a low-noise, CMOS PGA (gains 1 to 32), a ΔΣ modulator, and a programmable digital filter. The flexible analog front-end (AFE) incorporates two sensor-excitation current sources suitable for direct RTD measurement. A single-cycle settling digital filter maximizes multiple-input conversion throughput, while providing 130-dB rejection of 50-Hz and 60-Hz line cycle interference. The ADS1263 is available in a 28-pin TSSOP package and is fully specified over the –40°C to 125°C temperature range.

1.4.2 Hercules RM41L232

The RM41L232 device is a high-performance microcontroller for safety systems. The safety architecture includes dual CPUs in lockstep, CPU and Memory BIST logic, ECC on both the flash and the data SRAM, parity on peripheral memories, and loopback capability on peripheral I/Os. The RM41L232 device integrates the ARM Cortex-R4 CPU. The CPU offers an efficient 1.66 DMIPS/MHz, and has configurations that can run up to 80 MHz, providing up to 132 DMIPS. The device operates in little-endian (LE) mode.

1.4.3 TPS65381-Q1

The TPS65381-Q1 multi-rail power management IC (PMIC) supports Texas Instruments' TMS570LS series flash MCU and other MCUs with dual-core lockstep (LS) or loosely-coupled architectures (LC).

The TPS65381-Q1 device integrates multiple supply rails to power the MCU and an external sensor. An asynchronous-buck switch-mode power-supply converter with an internal FET converts the input battery voltage to a 6-V pre-regulator output. This 6-V pre-regulator supplies the other regulators. Furthermore, the device supports wake-up from ignition.

The device monitors undervoltage and overvoltage on all regulator outputs, battery voltage, and internal supply rails. A second band gap reference, independent from the main band gap reference, is used for the undervoltage and overvoltage monitoring, to minimize drifts in the main band gap reference from being undetected. In addition, regulator current-limits and temperature protections are implemented.

The TPS65381-Q1 has monitoring and protection functions, which includes the following: watchdog with trigger and modes, MCU error-signal monitor, clock monitoring on internal oscillators, self-check on the clock monitor, CRC on non-volatile memory, a diagnostic output pin allowing the MCU to observe the internal analog and digital signals of the device, a reset circuit for the MCU, and an enable drive output to disable the saving-path or external power-stages on detected faults. A built-in self-test (BIST) monitors the device functionality at start-up. A dedicated diagnostic state allows the MCU to check TPS65381-Q1 monitoring and protection functions.

1.4.4 REF5030

The REF5030 is a low-noise, low-drift, very high precision voltage reference. This reference is capable of both sinking and sourcing current, and has excellent line and load regulation.

1.4.5 SN6501

The SN6501 is a monolithic oscillator and power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

1.4.6 TPS62170

The TPS62170 is an easy to use synchronous step-down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology.It supports up to 0.5-A continuous output current at output voltages between 0.9 and 6 V (with 100% duty cycle mode) at a wide operating input range of 3 to 17 V.

1.4.7 TPS27082L

The TPS27082L IC is a high-side load switch that integrates a Power PFET and a control circuit in a tiny TSOT-23 package. The TPS27082L requires very low on-state quiescent current and offers very low off-state leakage, thus optimizing system power efficiency.

1.4.8 CSD18534Q5A

This 7.8-mΩ, 60-V, SON 5×6-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

1.4.9 ISO7141CC

The ISO7141CC provides galvanic isolation up to 2500 V_{RMS} for 1 minute per UL 1577 and 4242 V_{PK} per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, 566-V_{PK} working voltage. The ISO7141CC is a quad-channel isolator with three forward channels and one reverse-direction channel. This device is capable of a 50-Mbps maximum data rate with a 5-V supply and a 40-Mbps maximum data rate with a 2.7- or 3.3-V supply, with integrated filters on the inputs for noise-prone applications. The suffix CC states the default output state is high.

1.4.10 INA826

The INA826 is a low-cost instrumentation amplifier that offers extremely low power consumption and operates over a very wide single or dual supply range. A single external resistor sets any gain from 1 to 1000. It offers excellent stability over temperature, even at G > 1, as a result of the low gain drift of only 35 ppm/°C (max).

1.4.11 TLV333

The TLVx333 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the *zero-drift* family of amplifiers that uses a proprietary auto-calibration technique to simultaneously provide low offset voltage (15 µV, max) and near-zero drift over time and temperature at only 28 µA (max) of quiescent current. The TLVx333 family features rail-to-rail input and output in addition to near-flat 1/f noise, making this amplifier ideal for many applications and much easier to design into a system. These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V).

1.4.12 SN74LVC3G07

This triple buffer and driver is designed for 1.65- to 5.5-V V_{CC} operation. The output of the SN74LVC3G07 is open drain.

1.4.13 SN74LVC2G86

This dual two-input exclusive-OR gate is designed for 1.65- to 5.5-V V_{CC} operation.

1.4.14 SN74LVC1G332

The SN74LVC1G332 performs the OR function with three inputs in positive logic.

2 SafeTI™ Design Packages

This TI Design uses the SafeTI RM41L232 Hercules MCU. SafeTI components enable customers to develop their functional safety-related products. The RM41L232 is a member of the SafeTI product as part of the SafeTI Design Packages.

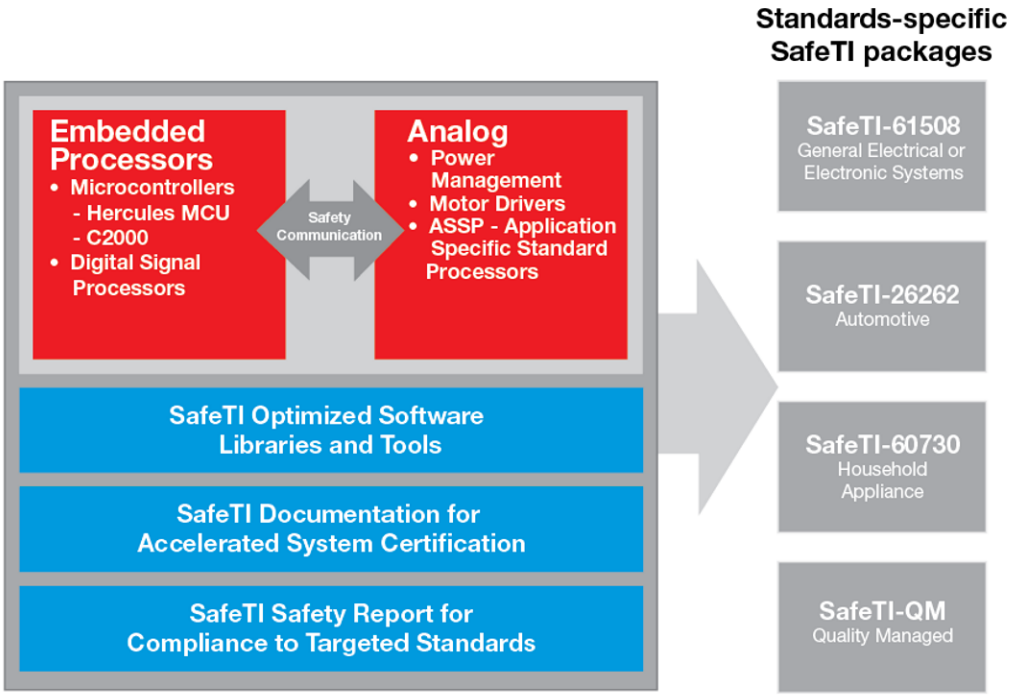

Figure 3. SafeTI Design Packages

SafeTI design packages for functional safety applications are used in a variety of safety-related applications, including industrial machinery, industrial processes, medical, automotive, rail, and aviation. SafeTI products help TI customers get to market quickly with safety-critical systems targeting compliance to safety standards such as ISO 26262, IEC 61508, and IEC 60730. SafeTI design packages help designers meet industry standard functional safety requirements while managing both systematic and random failures. Using SafeTI components helps customers achieve applicable end-product safety certification.

3 System Design Theory

3.1 Sensor Transmitter

A sensor transmitter converts an analog value from a sensor input to an equivalent 4- to 20-mA current. The loop current and the power for the sensor transmitter are transferred on the same pair of cables to enable easy installation in the field. To transmit a measurement value with current has advantages in terms of robustness in harsh environments as seen very often in the factory automation and control space.

As the name implies, the nominal current range is from 4 to 20 mA, but this design follows the NAMUR NE43 recommendation extending the range to 3.6 to 21 mA. A current outside these limits will be treated as failure.

3.2 AFE

This module features a dual 4- to 20-mA analog input to be used with sensor transmitters with 4- to 20-mA current loop interface. One or two (redundant) sensor transmitters are used for the same measured variable, such as temperature, pressure, and so on. In a non-safety environment, the two input channels can measure two independent measured variables. The three operating modes are (see also Figure 4):

- Sensor Configuration 1
  Two 4- to 20-mA loops measure redundantly the same analog variable side-by-side, or two separate 4- to 20-mA loops measure two different analog variables
- Sensor Configuration 2
  One 4- to 20-mA loop is measured by input channel 1 or 2 in a ping-pong manner

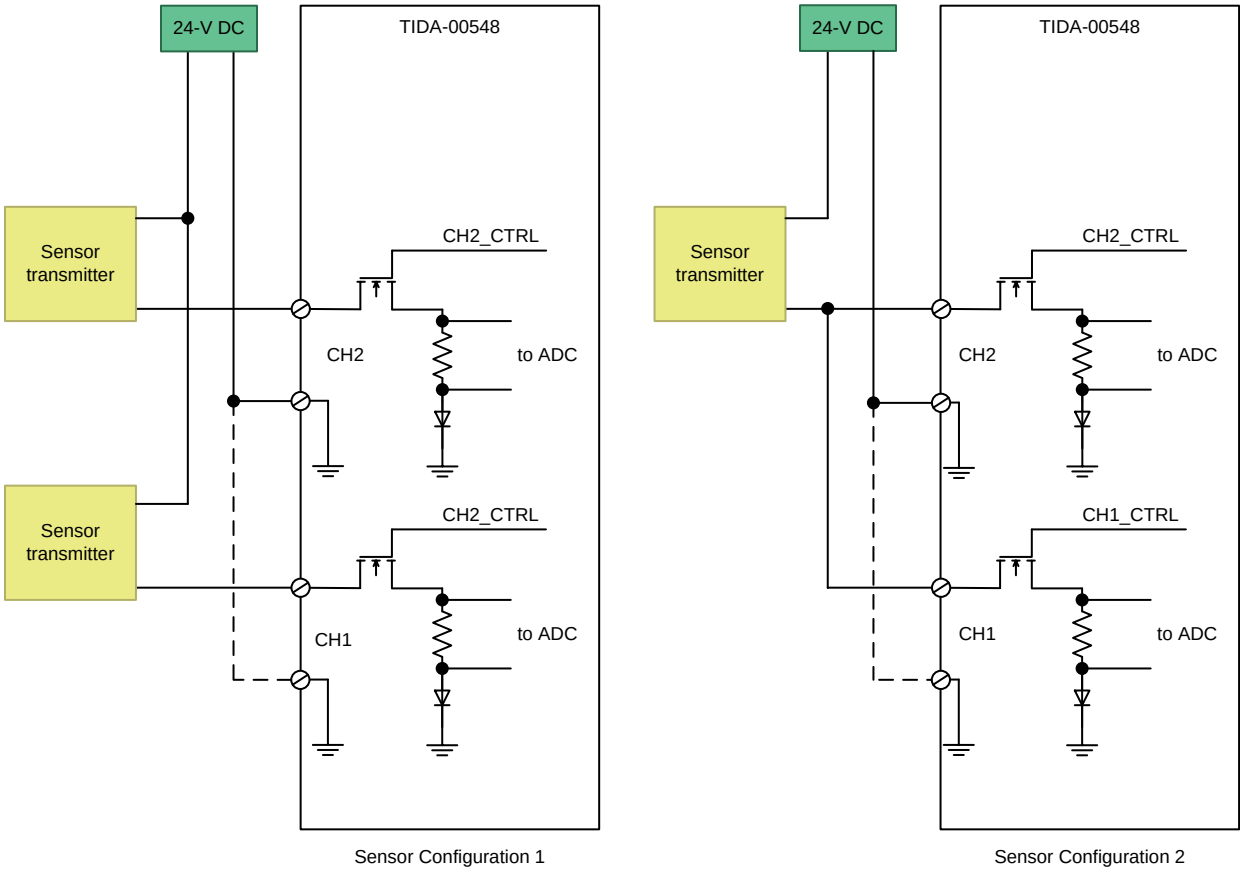

Figure 4. Sensor Connection

In Sensor Configuration 1, each sensor transmitter is constantly connected to a dedicated input while the internal multiplexer in the analog-to-digital converter (ADC) ADS1263 selects a channel for sampling. In case one signal chain fails, the converted voltage will differ from the other channel beyond a customizable tolerable deviation and is reported. Both input channel work 100% of the time, meaning signals *CH1_CTRL* and *CH2_CTRL* are always enabled.

In Sensor Configuration 2, only one sensor is used. Both analog inputs are connected in parallel. Only one channel is enabled at a time (with small overlap) while both channels will be switched on and off in a ping-pong manner. It is important to switch the *CH1_CTRL* and *CH2_CTRL* signals in a make-before-break scheme because both channels switched off at the same time would break the loop. When both channels are on, the voltage drop over the burden resistors is half the nominal value due to the two burden resistors in parallel.

For best performance, the input impedance (R_{ADCIN}) of the ADC channels is maximized to reduce the voltage drop over the protection resistors put in series in front of the inputs. R_{ADCIN} is dependent on the usage of the integrated programmable gain amplifier (PGA). If the PGA is disabled, R_{ADCIN} = 40 MΩ; if the PGA is enabled, R_{ADCIN} = 1 GΩ. The PGA is always enabled with a fixed gain of 1 V/V in this design. Higher PGA gains narrow the analog input range of the PGA towards midscale, which is not supported with this AFE. The ADS1263 unipolar power supply (A_{VDD} = 5 V, A_{VSS} = 0 V) and the enabled PGA limits the analog input range of $V_{AINP/N,MIN}$ = A_{VSS}+ 0.3 V = 0.3 V and $V_{AINP/N,MAX}$ = A_{VDD} – 0.3 V = 4.7 V. Diode D2 lifts AINN to a voltage greater than $V_{AINP/N,MIN}$ at the minimum loop current of 3.6 mA. D2 and the burden resistor value of 24.9 Ω directly lead to the analog input voltages given in Table 1.

Table 1. ADC Analog Input Voltages

I_{LOOP}	V_{DIODE}	V_{BURDEN}	VOLTAGE AT AINN	VOLTAGE AT AINP
3.6 mA	350 mV	90 mV	350 mV	440 mV
21 mA	600 mV	523 mV	600 mV	1123 mV

The analog input must be current limited to avoid excessive power dissipation of the burden resistor. The current-limiting component is an N-channel MOSFET. The gate-source voltage (V_{GS}) of the MOSFET controls the conductivity of the MOSFET. While the gate voltage (V_G) is held at 5 V, the source voltage of the MOSFET (V_S) varies with the voltage drop over the burden resistor and the diode. With the relationship V_{GS} = V_G – V_S, an increased V_S will lower V_{GS} and therefore lower the conductance of the MOSFET and the current is limited. V_G is connected to an AINx pin set to general-purpose output (GPO) functionality as it delivers a voltage of 5 V (A_{VDD}) when set to high. The resistor divider in front of the MOSFET gates is used to optimize the current limiter.

The maximum allowed continuous input current (I_{MAX}) is set by the maximum power dissipation of the burden resistor. For the resistor in 1206 package the maximum power dissipation is 0.25 W. Equation 1 calculates I_{MAX} based on the burden resistor value and its power dissipation:

$$I_{MAX} = \sqrt[2]{\frac{P}{R}} = \sqrt[2]{\frac{0.25\ W}{24.9\ \Omega}} = 100\ mA \quad (1)$$

The MOSFET CSD18534Q5A can dissipate up to 3.1 W. In case the field power supply of up to 36 V is connected to an input under worst conditions, the MOSFET dissipates around 36 V × 70 mA = 2.53 W in case the channel is enabled. The module disables the input channels in overcurrent condition, which can take several milliseconds. See also Section 4.3.

Open wires in a 4- to 20-mA loop is detected if no current flows through the burden resistor (no voltage drop). In a normal application the loop current is constantly measured, meaning such a failure will be detected immediately. Diode D2 prevents an uncontrolled current flow during reverse polarity connection. The inputs are protected against surge events. The high-voltage, pulse withstanding resistor directly at the inputs and the TVS diodes limit the power of an 8/20-µs surge ±1-kV (42-Ω) pulse IEC 61000-4-5 to an uncritical level for the ADS1263 inputs.

3.3 Analog Signal Conversion

The main purpose of this design is the reliable delivery of 4- to 20-mA loop current equivalent data samples. The system has seven main blocks involved in the analog-to-digital conversion. All blocks are redundant. Table 2 introduces the abbreviations and its description.

Table 2. Component Name Convention

NAME	DESCRIPTION
CH1	Input channel 1 (Burden is R17)
CH2	Input channel 2 (Burden is R25)
ADC1	32-bit ΔΣ ADC core (ADS1263)
ADC2	24-bit ΔΣ ADC core (ADS1263)
ADC3	12bit embedded SAR ADC core (Hercules)
INTREF	Internal 2.5-V reference (ADS1263)
EXTREF	External 3.0-V reference (REF5030)

With these components the analog signal can be converted with up to nine different paths. For best performance the combination CHx-ADC1-EXTREF is recommended. Figure 5 and Table 3 show path 6 (CH2-ADC1-EXTREF), which is used as default path throughout this document.

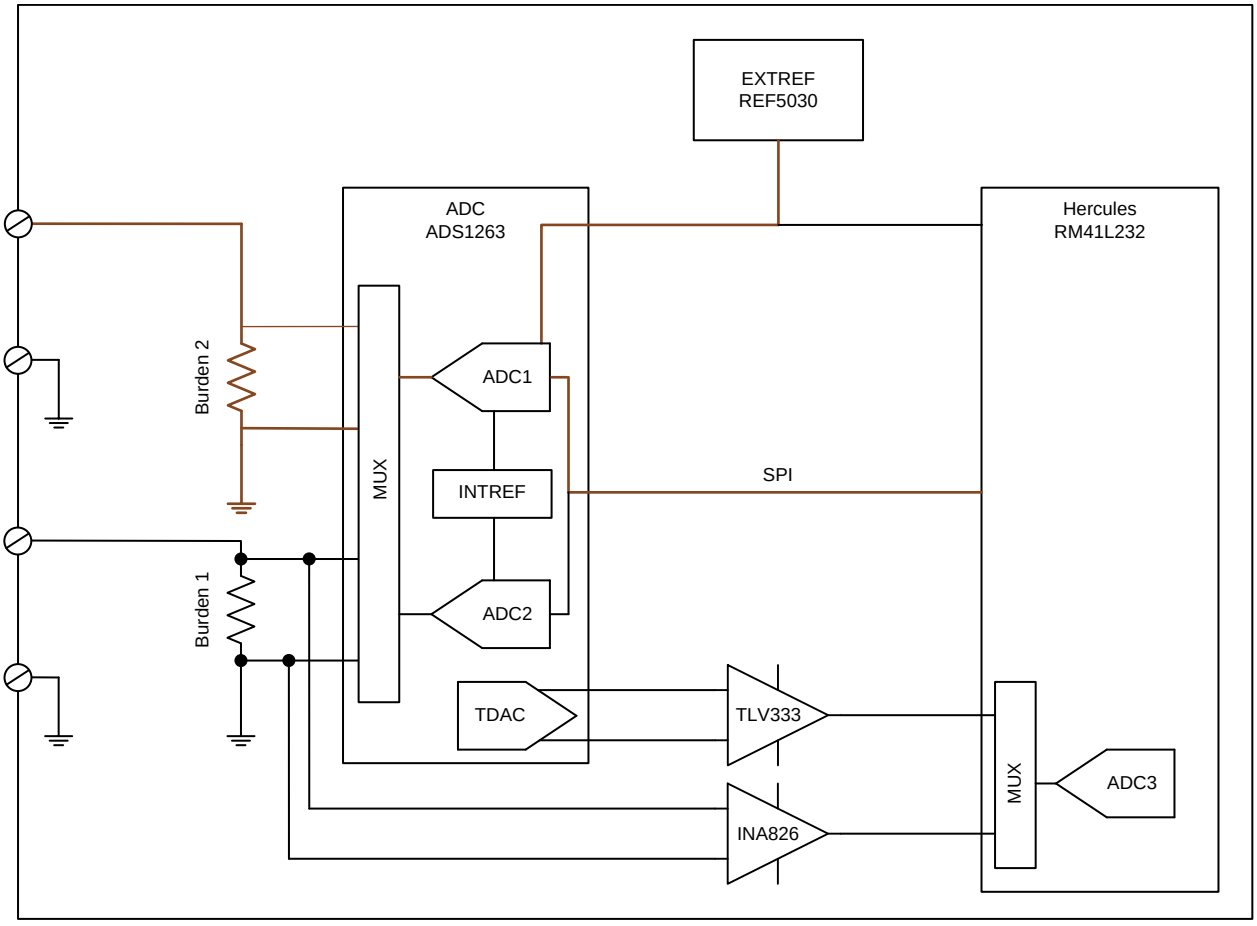

Figure 5. Default Analog Path

In Table 3, the column Possible Fails shows which components could be damaged in case the results of path 6 versus another path differ beyond a set limit. Column Performance shows the expected analog performance (A is best) for the particular path. While performance grades (PG) A to D are very close, path 5 is not meant to provide high-quality data samples; it is used for coarse estimation whether the output from the other paths are still in range. Path 5 is the only path independent from the ADS1263.

Table 3. Signal Paths

SIGNAL PATH	INPUT	ADC	REF	POSSIBLE FAILS	PERFORMANCE GRADE
1	Ch1	ADC1	EXT	Ch	A
2	Ch1	ADC1	INT	Ch, REF	C
3	Ch1	ADC2	EXT	Ch, ADC	B
4	Ch1	ADC2	INT	Ch, ADC, REF	D
5	Ch1	ADC3	EXT	Ch, ADC	Z
6	Ch2	ADC1	EXT	—	A
7	Ch2	ADC1	INT	REF	C
8	Ch2	ADC2	EXT	ADC	B
9	Ch2	ADC2	INT	ADC, REF	D

An error band is defined for each PG with PG A as reference. The error band of PG B, C and D are the same and specified as ±0.1%, for instance. For path 5, the error band needs to be relaxed.

3.4 Power

Power is provided from the PLC back end. Extensive surge protection is omitted since this is out of the scope of this TI Design. The drawback is the need of an isolated power supply. A push-pull topology is used due to its simplicity and low component count. The efficiency of the supply voltage at an input voltage of 5 V is 75%. The disadvantage of an unregulated output is compensated by the PMIC TPS65381Q1 (V_{IN} up to 36 V) and the DC/DC converter TPS62170 (V_{IN} up to 17 V). The transformer T1 has a ratio of 1:1.7. At the nominal input voltage of 5 V an output voltage range of 7.6 V is generated. The TPS65381Q1 generates an intermediate voltage of 6 V. The digital I/O voltage, V_{DIO}, of 3.3 V and the analog voltage, A_{VDD}, of 5 V are generated by internal LDOs from this 6 V. The Hercules core voltage, V_{CORE}, of 1.2 V can also be generated by the PMIC with an external MOSFET, which operates as LDO. The maximum core current is 145 mA. The MOSFET would need to dissipate (6 V – 1.2 V) × 145 mA = 696 mW. A more efficient approach is to use an external DC/DC converter. The TPS62170 dissipates 40 mW under same conditions.

The TPS27082L is the field-side power switch for the fail-safe isolator ISO7141FCC and controlled by the TPS65381Q1's ENDRV signal. If a fail occurs the TPS27082L will switch off the field-side power of the isolator. This pulls the SPI_MISO line on the host side of the isolator low. This exceptional condition notifies the host that communication is not possible until the SPI_MISO signal is set high again after a module restart, for instance.

3.5 Hercules and PMIC

The Hercules RM41L232 MCU is a component of the SafeTI design package, used to assist customers with their functional safety designs and designed to help our customers to meet functional safety standards such as ISO 26262, IEC 61508 and IEC 60730 . This dual-core lock step processor is the master to the ADS1263 over a SPI and slave to the back end through a second SPI. In addition, it constantly communicates over a third SPI to the TPS65381Q1. The integrated 12-bit SAR ADC with integrated 16-channel multiplexer is used to as an alternative analog path independent of the ADS1263. It uses the REF5030 as reference. The analog input range is 0 to 3 V. The voltage of burden resistor R17 and various system voltages are observed with this converter:

- Voltage over the burden resistor of channel 1 (signal *BURDEN1_SE*)
  The INA826 converts the differential signal to a single-ended signal. The gain of 5.61 V/V uses the full analog input range of 0 to 3 V with the maximum burden voltage drop of 523 mV (see also Table 1). The Hercules compares the data samples with the samples delivered from the ADS1263 (with limited accuracy). See also Section 4 for test results.
- Test DAC (TDAC) voltage (signal *TDAC_SE*)
  The TDAC integrated in the ADS1263 provides a programmable differential voltage to the multiplexer input of the ADS1263 and to pins AIN6 (V+) and AIN7 (V–). The Hercules ADC converts the voltage to verify correct TDAC operation. The TLV333 converts the differential signal (max. 4 V) to a single-ended signal and gains it by –3.5 dB.
- ADS1263 internal voltage reference (signal *ADS_REF*)
  The internal reference of the ADS1263 is observed with this input. Regardless of the ADS1263 reference input source (internal or external) the voltage reflects always the internal reference of 2.5 V when the internal reference turned on.
- Supply voltage monitor (signal *SUPPLY_MON*)
  The main supply voltage of the module is observed with this input. A 1:3 resistor divider attenuates the nominal voltage of 7.6 to 2.53 V.
- Offset measurement (GND)
  The converted value of this input is deducted from the *ADS_REF* and *SUPPLY_MON* converted analog signal for offset compensation. Signals *BURDEN1_SE* and *TDAC_SE* include active components, which must be included in offset compensation by setting the sensed signal to zero.

The ERROR pin of the RM41L232 indicates to the TPS64381Q1 that an error occurred on the Hercules. The fault conditions are software programmable. The ENDRV pin of the TPS64381Q1 indicates that either the RM41L232 or the TPS64381Q1 itself faces a failure. The ENDRV pin controls the load switch TPS27082L.

3.6 Self-Test Capabilities

The ability to periodically self-test critical components in the system is an essential feature of a safety design. As more components can be tested as higher the diagnostic coverage (DC). The Hercules RM41L232 has extensive self-test features already built-in. The test of other critical components in the system is the responsibility of the system designer of the end product. The self-test is performed either by the stimulation of a component with a known input or by the comparison of results of redundant components.

An example of stimulation is the usage of the integrated test DAC in the ADS1263. A programmable differential output voltage is applied to ADC1 and ADC2. To verify the test DAC output the correct voltage it is also fed through TLV333 to ADC3.

An example of comparison is to convert the input signal by at least two signal paths (see also Section 3.3). If the output codes differ a failure of at least one component is uncovered. The faulty component is revealed when certain combinations (different paths) are tested (see also Table 3). Power fails and internal self-test fails would immediately result in the transition to the safe state. If the signal chain recognizes anomalies, it is the user's responsibility to take action. Table 4 shows how critical components can be tested.

Table 4. Hardware Self-Test

COMPONENT TO TEST	PART NUMBER	VERIFIED BY	RESULT ON FAILURE	SAFE STATE
Hercules	RM41L232	self	Isolator shutdown	YES
PMIC	TPS65381	self	Isolator shutdown	YES
ADC1	ADS1263	ADC2, ADC3, TDAC	Wrong output	custom
ADC2	ADS1263	ADC1, ADC3, TDAC	Wrong output	custom
ADC3	RM41L232	ADC1, ADC2, TDAC	Wrong output	custom
INT REF	ADS1263	EXT REF	Wrong output	custom
EXT REF	REF5030	INT REF	Wrong output	custom
CH1	Burden 1	CH2	Wrong output	custom
CH2	Burden 2	CH1	Wrong output	custom
TDAC op amp	TLV333	ADC1, ADC2, ADC3	Wrong output	custom
CH1 op amp	INA826	ADC1, ADC2, ADC3	Wrong output	custom
Load switch	TPS27082L	Hercules	No or always communication	YES
Isolator	ISO7141FCC	Load Switch	No communication	YES
V_{CORE} generation	TPS62170	—	No communication	YES
Main voltage	SN6501	—	No communication	YES

3.7 Monitoring and Diagnostics

Monitoring is a way to passively ensure a measured variable is within its limits. The observation of all supply voltages in the system is a good example. If any voltage is outside its limits, the correct behavior of the entire system operation cannot be assured anymore. The PMIC TPS65381Q1 monitors all supply voltage and takes appropriate actions.

The PMIC observes the Hercules processor with an intelligent watchdog scheme over SPI. The PMIC sends a question and the Hercules has to send back four answers in a defined time frame.

3.8 Signaling

The TIDA-00548 provides four LEDs for status indication. These LEDs are visible at the terminals using optical fiber channels. Table 5 explains the purpose of each LED.

Table 5. LED Assignment

LED	COLOR	LED ON	LED OFF
1	Green	Main voltage present	Main voltage absent
2	Red	Isolator powered down (safe state)	Isolator powered up
3	Red	Hercules reports fault	Hercules normal operation
4	Red	User defined	User defined

The LEDs in Figure 6 indicate that the main power is applied and the user LED is enabled (LED1 to LED4 from left to right).

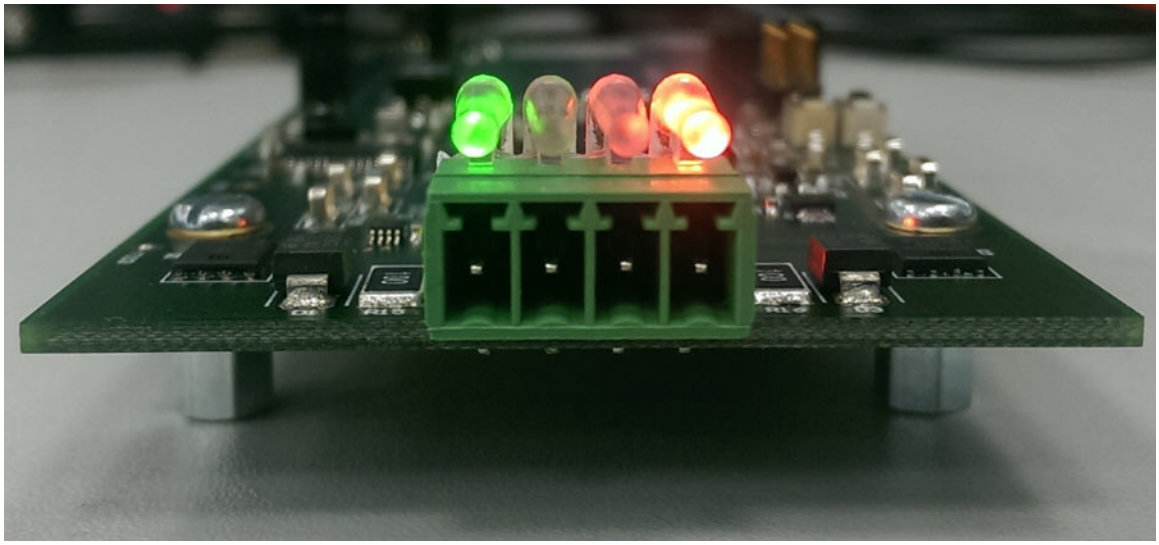

Figure 6. LED Indication

4 Testing and Results

This section discusses the setup, testing, and results of the TIDA-00548 hardware. The test software (not provided) for the Hercules processor tests all functionality and runs performance measurements of the analog signal chain. The integrated development environment for the software is Code Composer Studio™ (CCS) version 6.0.1. For all tests, the data samples are stored in the RM41L232 internal memory during the test run. The results are then saved to the hard disc drive with the *Save Memory* feature of CCS for further processing using Microsoft® Excel®.

4.1 Effective and Noise-Free Bits

To obtain the effective and noise-free bits the standard deviation is calculated from 200 samples taken from an externally applied 12-mA constant current. The loop current is not measured by an external DMM since the absolute value is not of importance. It is important that the current does not drift during data acquisition. Figure 7 shows the hardware setup.

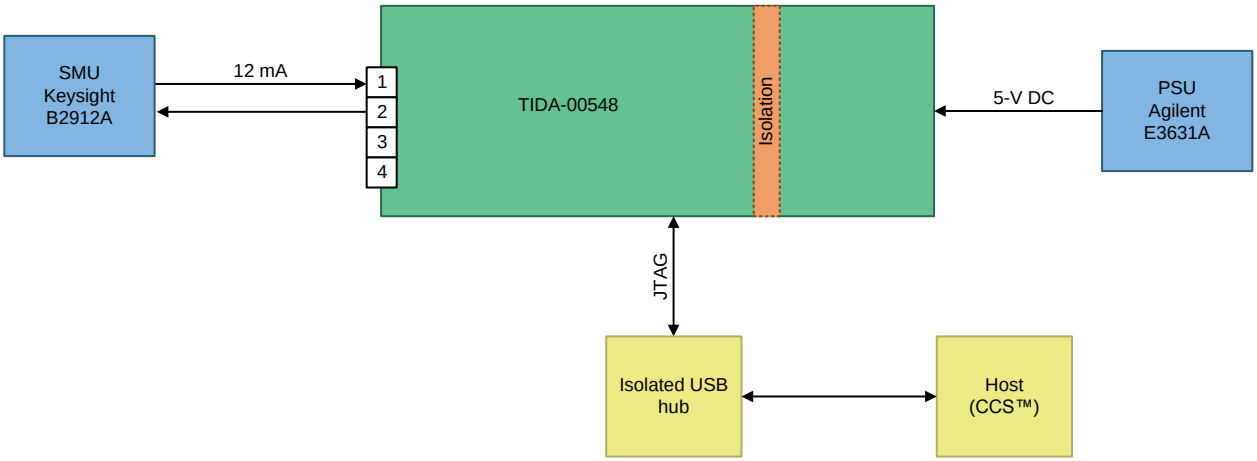

Figure 7. Test Setup for Effective and Noise-Free Bits Measurement

The effective number of bits and the noise-free bits are calculated using Equation 2 and Equation 3:

$$\text{Effective bits} = \log_2\left(\frac{2^N}{\text{stddev}\left[\text{samples}\right]}\right) \quad (2)$$

where N = data width of converter

$$\text{Noise-free bits} = \log_2\left(\frac{2^N}{\text{stddev}\left[\text{samples}\right]\times 6.6}\right) = \text{Effective bits} - 2.72\,\text{bits} \quad (3)$$

Three different signal paths (see Table 3) are tested to show their performances and limitations.

4.1.1 Performance of Path 6: CH2-ADC1-EXTREF

Path 6 is the default analog path with the best analog performance. The 32-bit converter (ADC1) of the ADS1263, the high-performance external reference REF5030 and input channel 2 are used. The code-to-current calculation for this path is:

$$I_{PATH6} = \frac{\left(\frac{\text{code}}{2^{N-1}}\times V_{EXTREF}\right)}{R_{BURDEN}} = \frac{\left(\frac{\text{code}}{2^{31}}\times 3\,V\right)}{24.9\,\Omega} \quad (4)$$

Figure 8 shows the histogram. The peak-to-peak variation is about 600 nA with an uncalibrated system offset of about 17 µA.

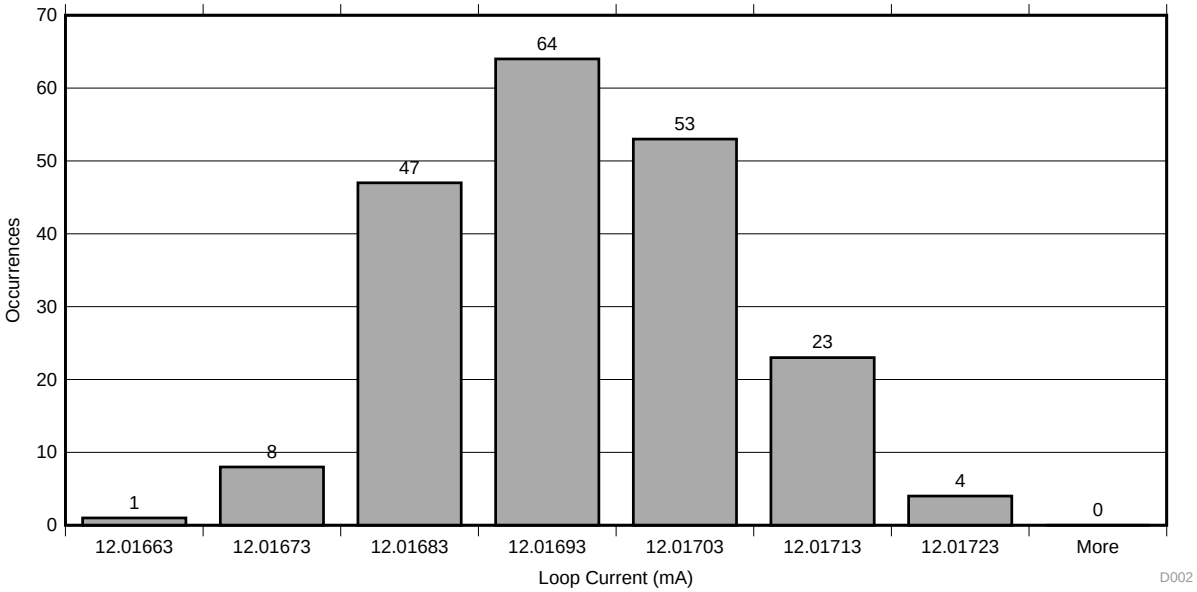

Figure 8. Histogram 32-bit ADC With External Reference

The histograms translates to *20.03 effective number of bits* (derived from the standard deviation) and to *17.31 noise-free bits*. The noise-free bits are obtained from 6.6x standard deviation. This equates to 99.9% of the samples.

4.1.2 Performance of Path 7: CH2-ADC1-INTREF

This analog signal path uses the same ADC core and input channel, but with the built-in reference. If the results of the internal reference as shown in Figure 9 satisfy the system requirements, a lower cost reference can be used instead. The internal reference will eventually perform better then, which makes path 7 the default path. The code-to-current calculation for this path is:

$$I_{PATH7} = \frac{\left(\frac{code}{2^{N-1}} \times V_{INTREF}\right)}{R_{BURDEN}} = \frac{\left(\frac{code}{2^{31}} \times 2.5\ V\right)}{24.9\ \Omega} \quad (5)$$

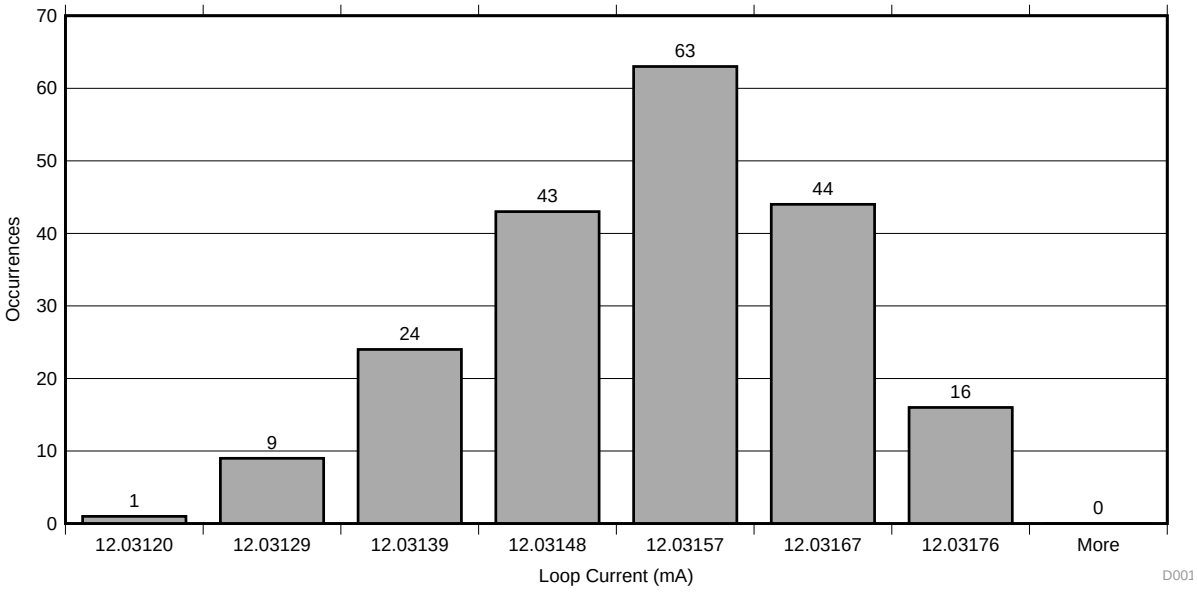

Figure 9. Histogram 32-bit ADC With Internal Reference

In this path slightly less performance is expected due to lower performance of the internal reference versus the external reference. The obtained 19.68 effective number of bits and 16.96 noise-free bits are still close to performance of path 6.

4.1.3 Performance of Path 5: CH2-ADC3-EXTREF

An analog signal path independent to the ADS1263 is provided with the embedded 12-bit SAR ADC built-in the RM41L232 Hercules microcontroller. The RM41L232 requires an external reference. The performance is lower due to the limited number of bits, but sufficient to verify that the data samples from the ADS1263 are in the ball park. The code-to-current calculation for this path takes the gain of the INA826 into account:

$$I_{PATH5} = \frac{\frac{code}{2^N} \times V_{EXTREF}}{Gain[INA826] \times R_{BURDEN}} = \frac{\frac{code}{2^{12}} \times 3\ V}{\left(1 + \frac{49.4\ k\Omega}{10.7\ k\Omega}\right) \times 24.9\ \Omega} \quad (6)$$

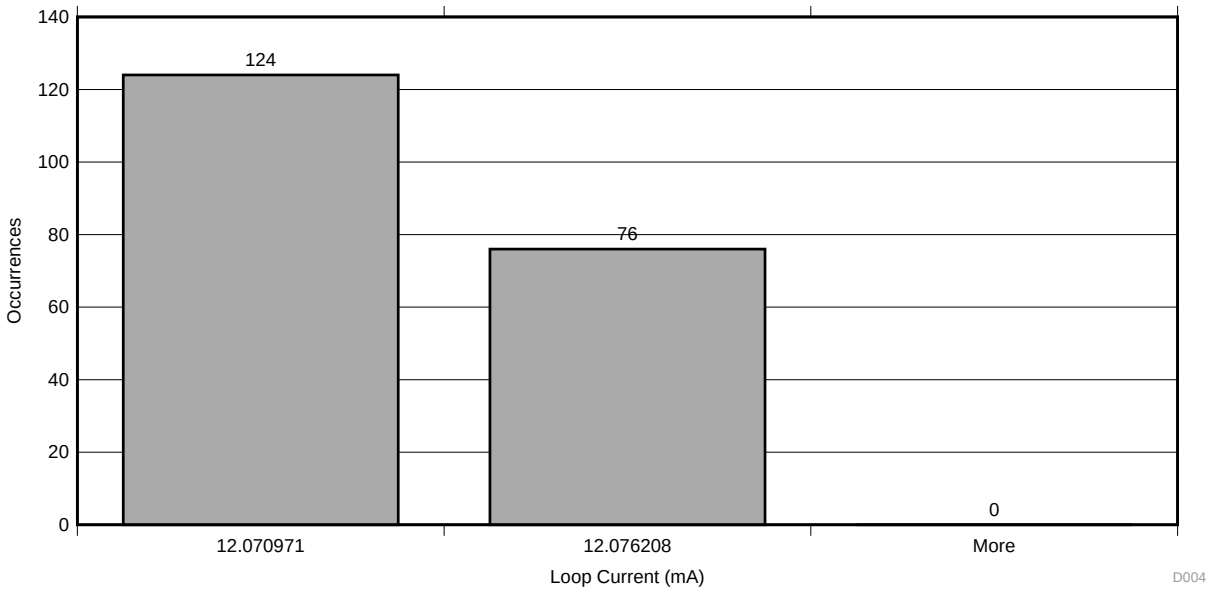

Figure 10. Histogram 12-bit ADC Embedded in Hercules

Due to the relatively low 12-bit resolution, the histogram consists of two bins only. The resulting 13.04 effective number of bits and 10.32 noise-free bits are in the expected range. Like for the high-performance paths, it is recommended to compensate the offset error of the converter. To get the offset, path 5 is measured with open connection (no current flow). During the test, a value of 0x000F was observed. Calculating the phantom current with Equation 6 leads to 78.5 µA (code = 0x000F), which is about the offset to the 12 mA given in Figure 10.

4.2 Error Over Analog Input Range

The full-scale error is commonly used today across specifications of PLC modules to show the error of the measured data sample to the real current. The high-performance path 6 is used for this measurement (see Table 3). Figure 11 shows the test setup.

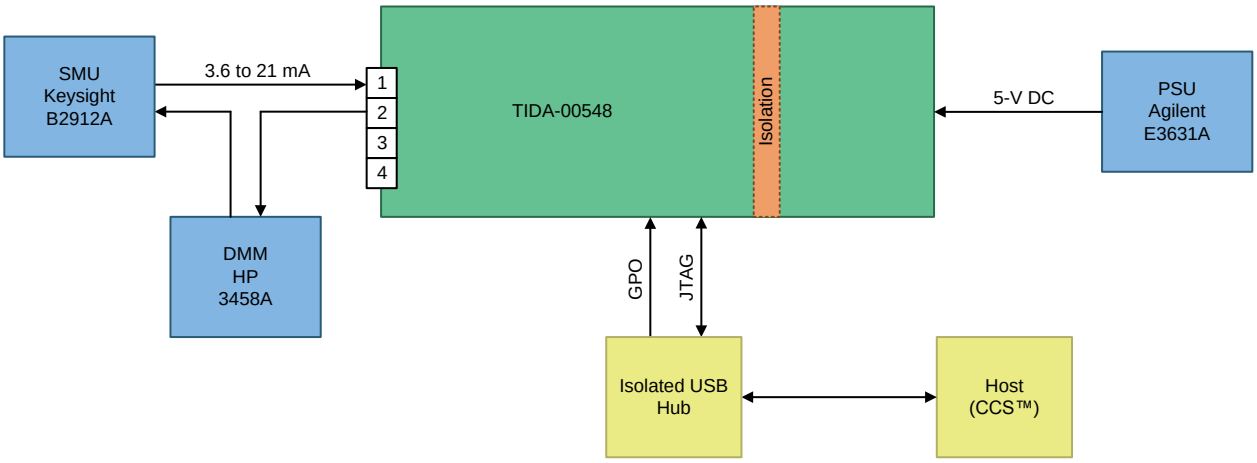

Figure 11. Test Setup for Full-Scale Error Measurement

The 8.5-digit DMM HP3458A measures the current through the loop and is used as reference. The ADC data samples are used to back-calculate the current the module actually sees. Prior to the actual measurement the offset correction code is obtained by averaging 16 samples without wires connected to the terminals (see Equation 7). This *cold* offset calibration can be performed during functional test without additional effort in the manufacturing process.

$$I_{MODULE} = \frac{\left(\frac{code - offset}{2^{N-1}} \times V_{EXTREF}\right)}{R_{BURDEN}} = \frac{\left(\frac{code - offset}{2^{31}} \times 3\ V\right)}{24.9\ \Omega} \quad (7)$$

The full-scale error is:

$$E_{FS[\%]} = \frac{abs\left(I_{DMM} - I_{MODULE}\right)}{0.021\ A} \times 100 \quad (8)$$

In this design, $E_{FS[\%]}$ does not exceed ±0.009% at 25°C as shown in Figure 12. The measured current range is 3 to 21 mA in steps of 25 µA.

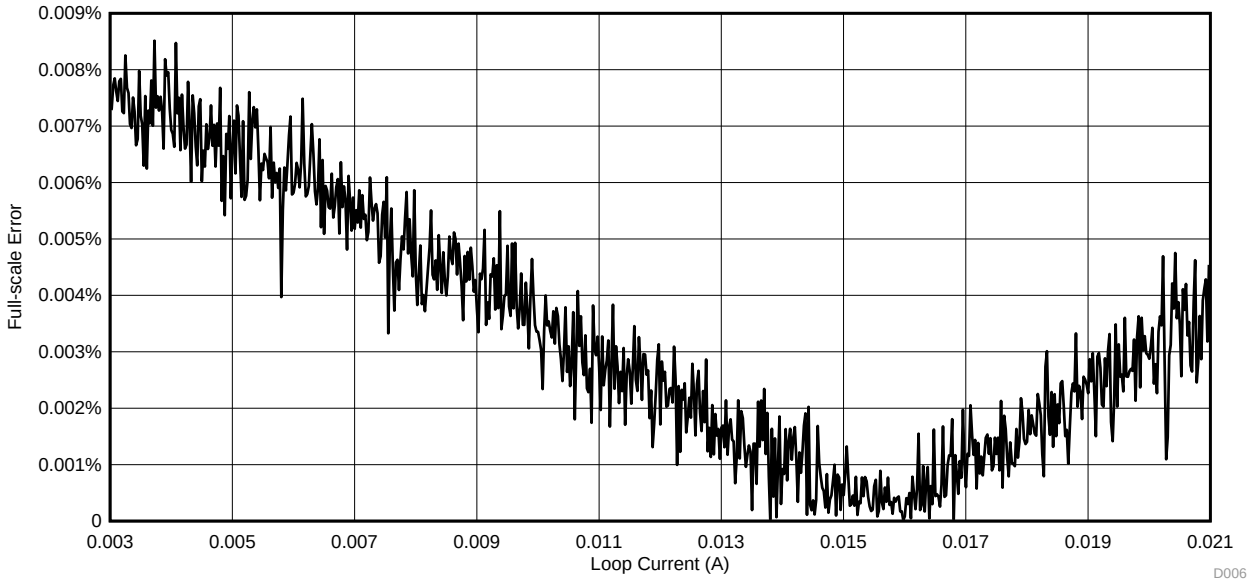

Figure 12. Full-Scale Error for Path 6

4.3 Analog Input Current Limiter Performance

The input current limiter is an important part to protect the module against extensive current flow into the module. It is designed to withstand continuous 33 V at the terminals. Section 3.2 describes the current limiter function. In case of a worst case failure where the maximum allowed input voltage of 33 V is continuous connected to an input (while the input is enabled), an input current of 100 mA is measured. Under normal working conditions, the maximum input current of 21 mA causes a voltage drop at the input terminal of 1.3 V.

5 Design Files

5.1 Schematics

To download the schematic, see the design files at TIDA-00548.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00548.

5.3 PCB Layout Recommendations

5.3.1 Layer Plots

To download the layout prints, see the design files at TIDA-00548.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00548.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00548.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00548.

6 Trademarks

7 About the Author

LARS LOTZENBURGER is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Lars brings to this role his extensive experience in analog/digital circuit development, PCB design, and embedded programming. Lars earned his diploma in electrical engineering from the University of Applied Science in Mittweida, Saxony, Germany.

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