

NOTES, UNLESS OTHERWISE SPECIFIED:

- 1. The netname "DMD\_P3P3V" represents connection to the +3.3V digital power plane.
- 2. The symbol  $\equiv$  represents connection to the digital ground plane.
- 3. A "Z" suffix on a signal name indicates an active low signal.
- 4. All components with designators "U", "D", "Y" and "Q" are electrostatic discharge sensitive.
- 5. All resistor values are in ohms, 1/16W and 5% unless otherwise specified.

HIGHEST REFERENCE DESIGNATORS USED						
C103	D5	J4	L5	R56	TP31	U7
Q9						



COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY			
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	Initial Release	7/15/2020	

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		ENGR Amy White	3/9/2015		
		SYST			
		PRJ John O'Connor	3/9/2015	TITLE DLPLCR67EVM - DLP041	
		QA			
NEXT ASSY	USED ON			D DRAWING NO 2514417	REV A
APPLICATION		SW Cadence 16.6		SCALE	SHEET 1 of 7

J1 & J2

Input Flex  
Connector

From  
Slave  
ASIC

From  
Master  
ASIC

A/B DMD DATA (DD AP[15:0], DD AN[15:0], DD BP[15:0], DD BN[15:0])

A/B DMD CLK (DCLK AP, DCLK AN, DCLK BP, DCLK BN)

A/B SCTRL (SCTRL AN, SCTRL AP, SCTRL BN, SCTRL BP)

C/D DMD DATA (DD CP[15:0], DD CN[15:0], DD DP[15:0], DD DN[15:0])

C/D DMD CLK (DCLK CP, DCLK CN, DCLK DP, DCLK DN)

C/D SCTRL (SCTRL CN, SCTRL CP, SCTRL DN, SCTRL DP)

DAD CONTROL (STROBE, MODE[1:0], SEL[1:0], ADDR[3:0], OEZ)

SCP CONTROL (CLK, DO, DI, ENZ, IRQZ)

DMD RSTZ

U5, U6, U7  
Level Translators  
3.3V->1.8V

U1  
VREG  
3.3V->1.8V

3.3V

U2

DMD Power Supplies

VOFFSET

VBIAS

VRESET

PG OFFSET

EN OFFSET

U3

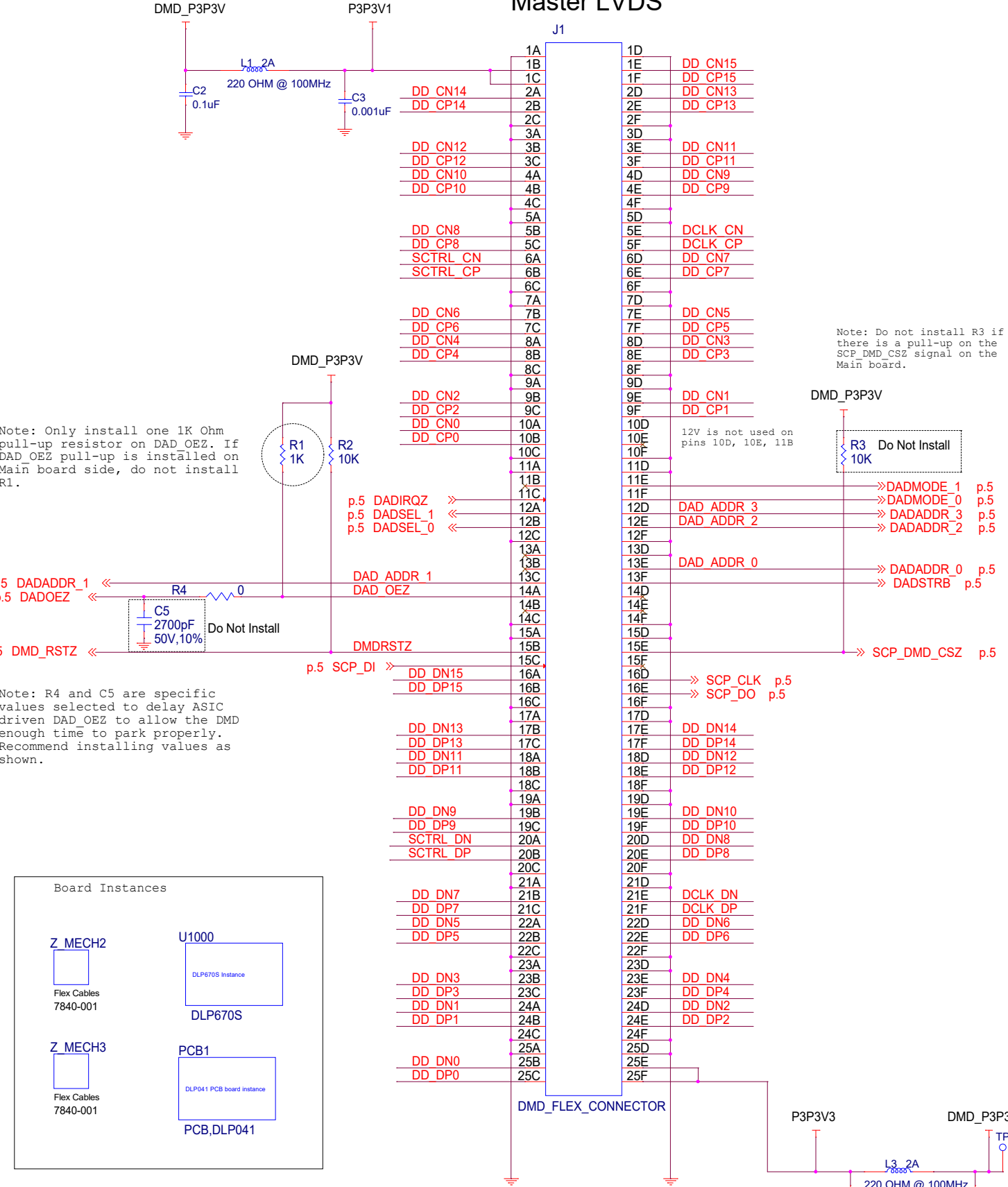
DLP670S

PAGE 3

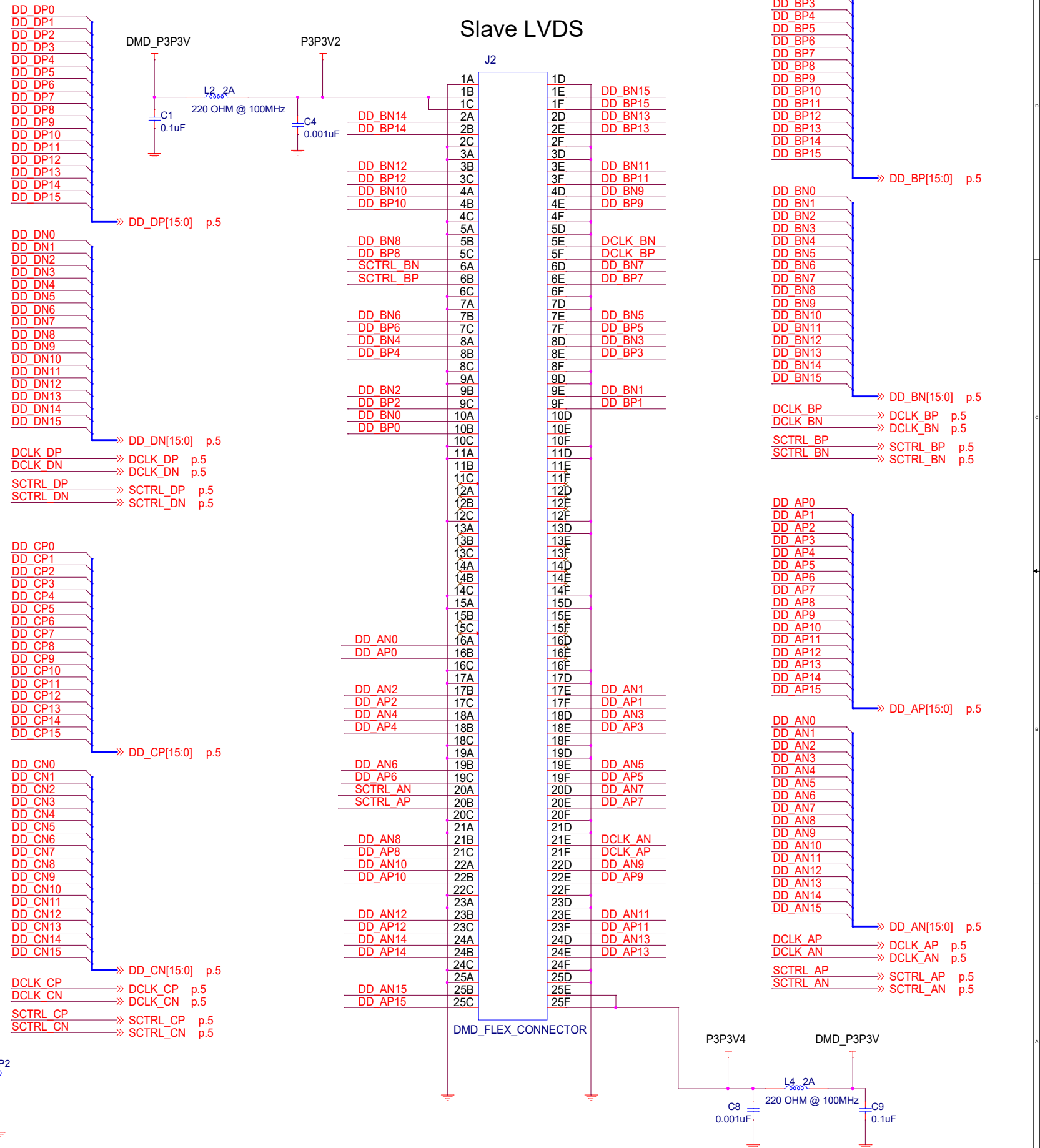
PAGE 4

PAGE 5 & 6

Master LVDS

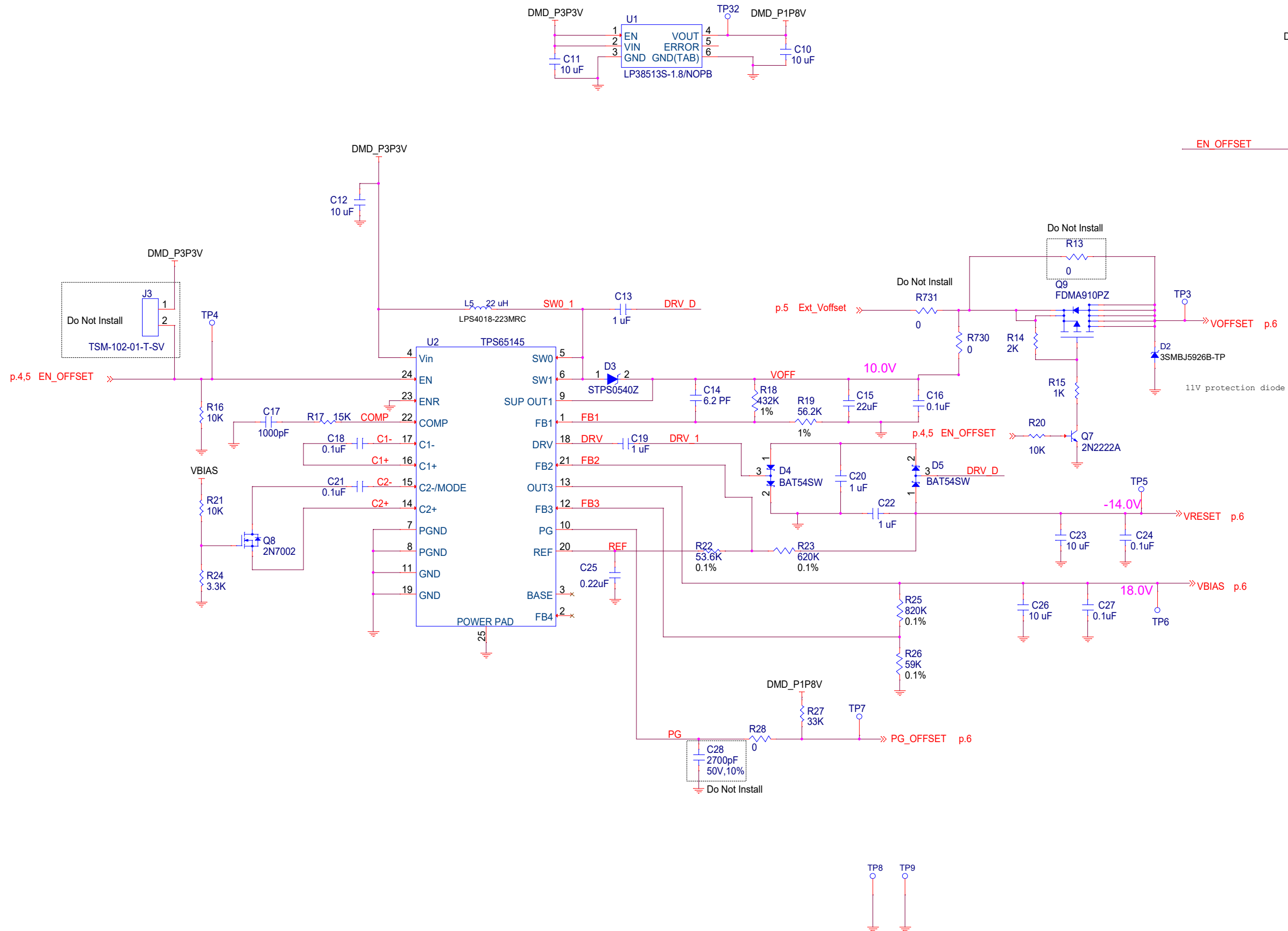
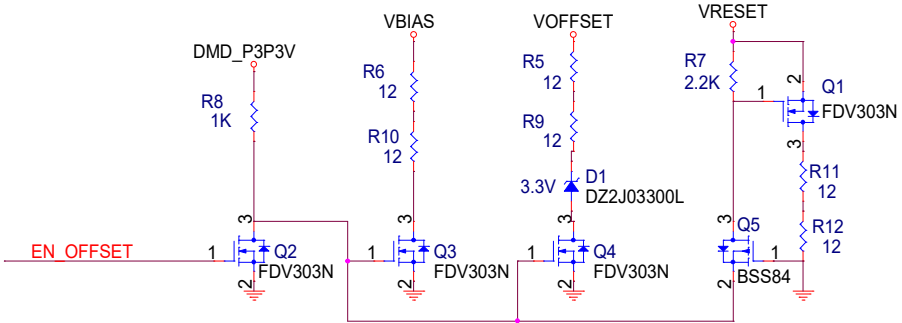


Slave LVDS



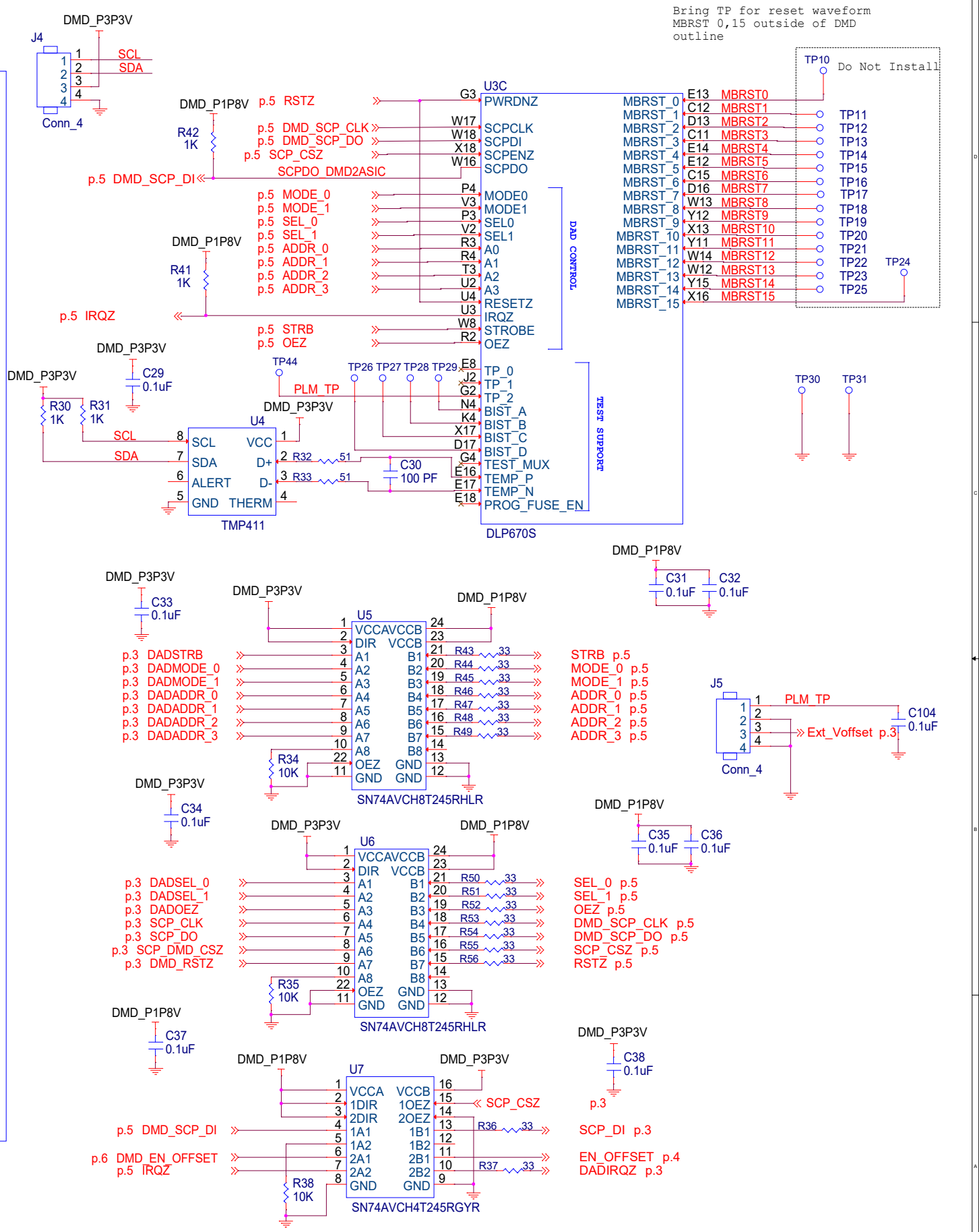
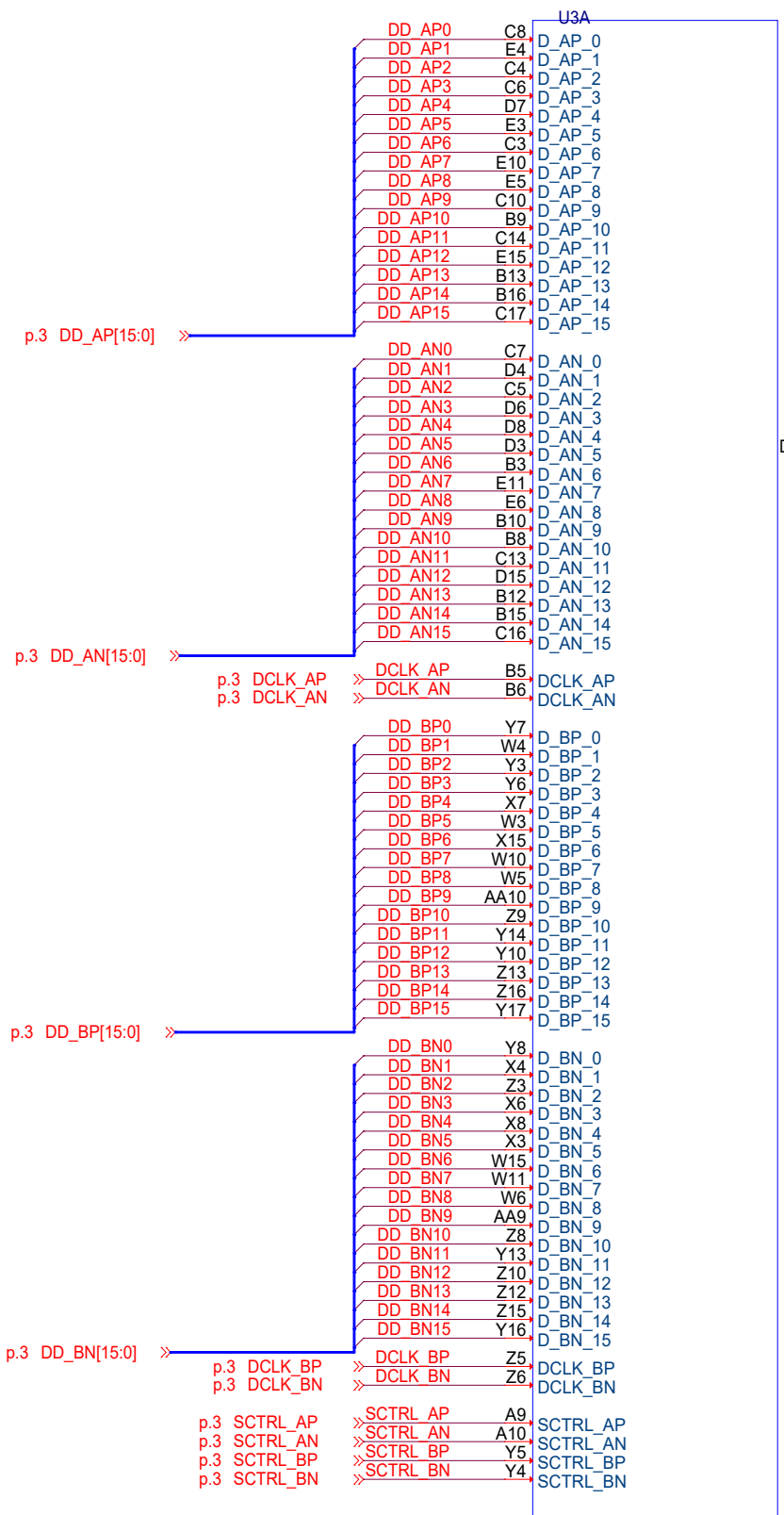
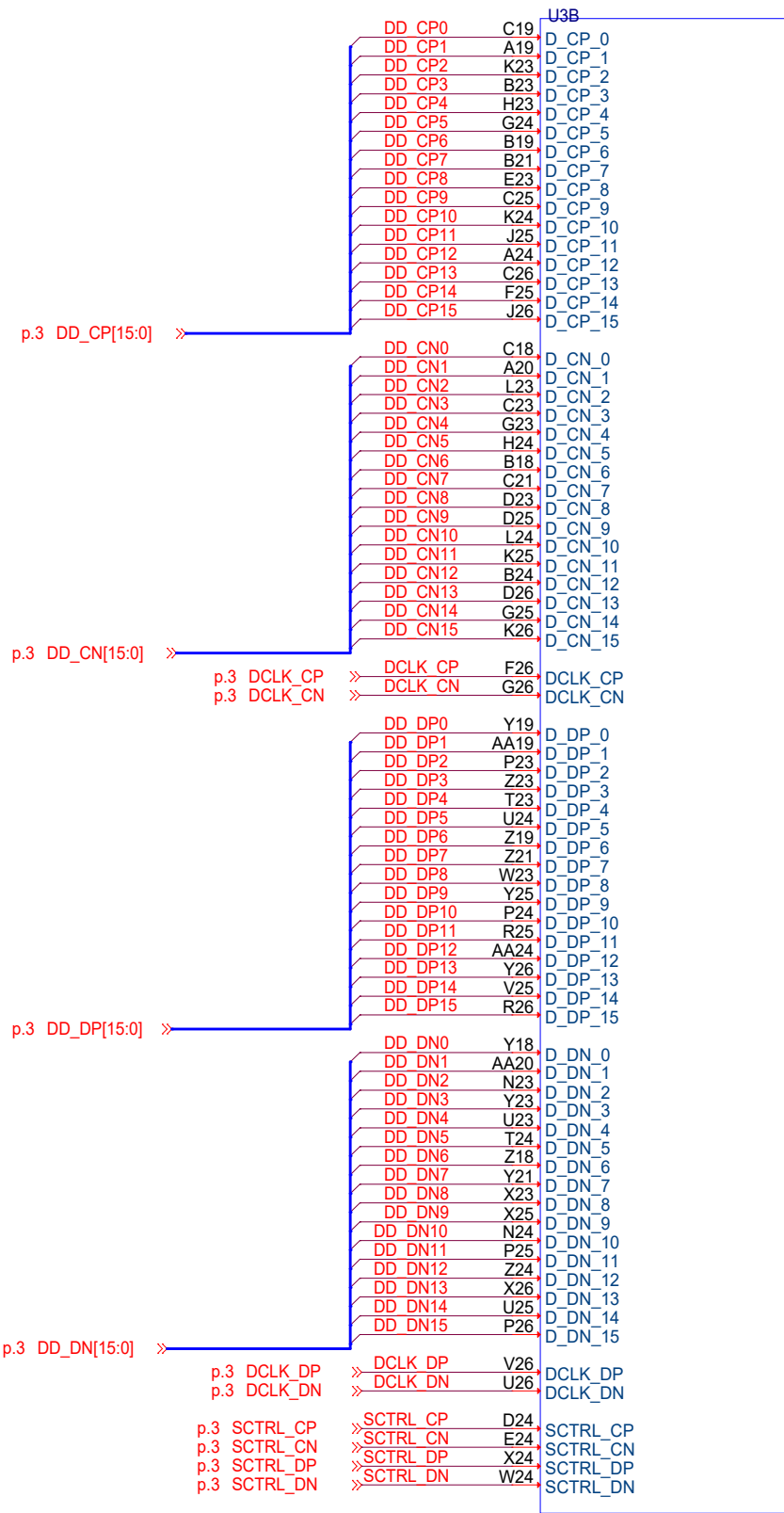
INPUT CONNECTOR

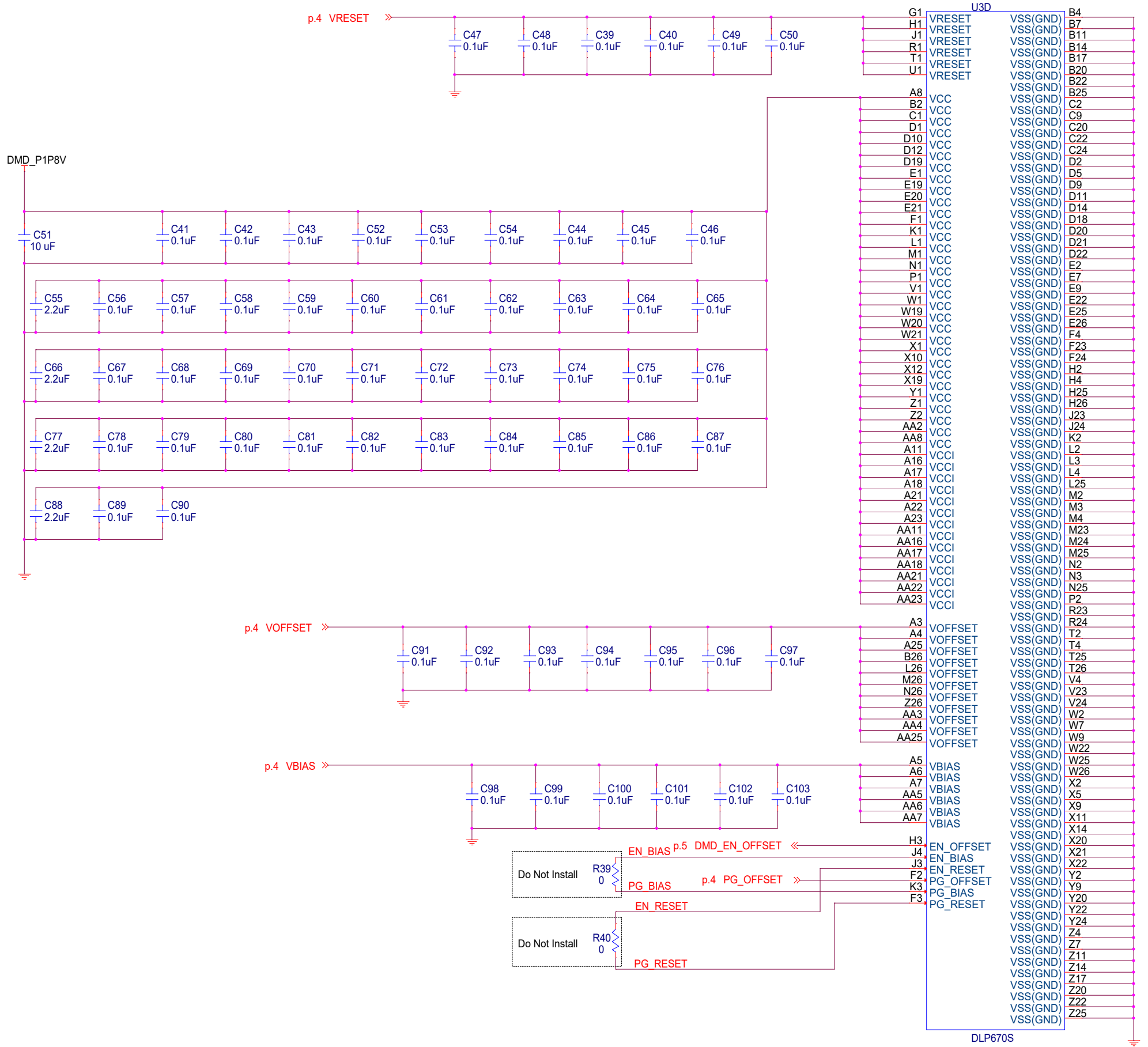
# Power Down Circuitry



# DMD Power Supplies







# DMD Power/Gnd

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