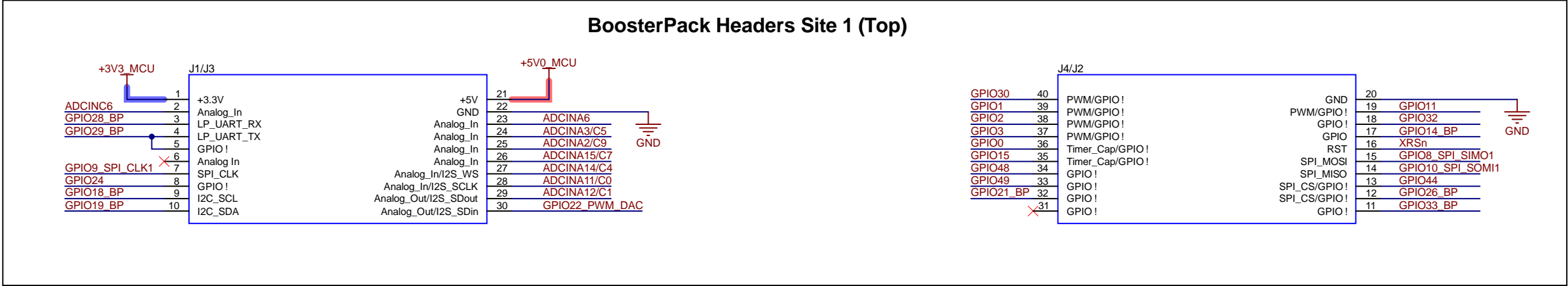




A



UART Routing

SCI_SEL1	SCI_SEL2	GPIO28/29 Route	GPIO23/40 Route
0	0	XDS110 COM Port	BP
0	1	XDS110 COM Port	NC
1	0	BP	BP
1	1	BP	XDS110 COM Port

- DEFAULT

The schematic diagram illustrates the UART routing for three TS5A23157DGSR multiplexers (U3, U4, U9) and an SPDT switch (S2). The routing is configured for the default settings (SCI_SEL1=0, SCI_SEL2=0).

U9 (TS5A23157DGSR) Connections:

- V+ (8) to +3V3_MCU
- COM1 (10) to GPIO28 (100000pF capacitor to GND)
- IN1 (1) to SCI_SEL1
- COM2 (6) to GPIO29
- IN2 (5) to SCI_SEL1
- NC1 (9) to GPIO28_SCIRX
- NO1 (2) to GPIO28_BP (-J1_3)
- NC2 (7) to GPIO29_SCITX
- NO2 (4) to GPIO29_BP (-J1_4/5)
- GND (3) to GND

U3 (TS5A23157DGSR) Connections:

- V+ (8) to +3V3_MCU
- COM1 (10) to GPIO40 (100000pF capacitor to GND)
- IN1 (1) to SCI_SEL2
- COM2 (6) to GPIO23
- IN2 (5) to SCI_SEL2
- NC1 (9) to GPIO40_BP (-J5_44/45)
- NO1 (2) to GPIO40_SCITX
- NC2 (7) to GPIO23_BP (-J5_43)
- NO2 (4) to GPIO23_SCIRX
- GND (3) to GND

U4 (TS5A23157DGSR) Connections:

- V+ (8) to +3V3_MCU
- COM1 (10) to MCU_TXD (100000pF capacitor to GND)
- IN1 (1) to SCI_SEL1
- COM2 (6) to MCU_RXD
- IN2 (5) to SCI_SEL1
- NC1 (9) to GPIO29_SCITX
- NO1 (2) to GPIO40_SCITX
- NC2 (7) to GPIO28_SCIRX
- NO2 (4) to GPIO23_SCIRX
- GND (3) to GND

S2 (SPDT) Connections:

- 1 to 4
- 2 to 5
- 3 to 6
- 1, 2, 3 to +3V3_MCU
- 4, 5, 6 to GND

Oscillator

Route cleanly and place near U1

XTAL_X2

1

3

XTAL_X1

C2 12pF

GND

R10 0

GPIO18_X2

R12 0

- J5_49 GPIO18_BP

Y1

2

4

GND

R11 0

GPIO19_X1

R13 0

- J5_50 GPIO19_BP

C3 12pF

GND

By default:


- Crystal Y2 is connected between GPIO18_X2 and GPIO19_X1.
- GPIO18_BP AND GPIO19_BP are connected to the BoosterPack headers.

If GPIO18 and GPIO 19 are needed at the Boosterpac k Headers:

- Remove R10 and R11, populate R12 and R13 with 0 ohm resistors
- The F280015x device's internal oscillator will need to be used

XROSC Ext Comps

Keep trace short as possible
Place near X1 pin



The diagram shows a circuit trace starting from a pin labeled **GPIO19_X1**. The trace splits into two parallel branches, each leading to a component connected to ground (GND). The first branch contains a capacitor labeled **C16** with values **10nF** and **6V** indicated. The second branch contains a resistor labeled **R20** with a value of **100k**. Both components are marked with a large red 'X', indicating they should be removed. A blue dashed box encloses the entire circuit area. Text to the left of the diagram states: 'Keep trace short as possible' and 'Place near X1 pin'.

CAN Routing

The diagram illustrates the CAN routing configuration. A DPDT switch, controlled by S4, routes signals between J8_71 and J8_72. The routing is as follows:

- J8_71 GPIO5_BP (6) is routed to J8_72 GPIO4_BP (3).
- J8_71 GPIO5 (5) is routed to J8_72 GPIO4 (2).
- J8_71 GPIO5_CANRX (4) is routed to J8_72 GPIO4_CANTX (1).

SPI Routing

The diagram illustrates the routing for three SPI signals. For GPIO9, the signal is routed to J1_7 via R22, while the alternative path to J5_47 via R80 is crossed out. For GPIO8, the signal is routed to J2_15 via R81, while the alternative path to J6_55 via R84 is crossed out. For GPIO10, the signal is routed to J2_14 via R79, while the alternative path to J6_54 via R82 is crossed out. All resistors are labeled with a value of 0.

Boot Mode Select

The diagram illustrates the Boot Mode Select circuit. It features an SPDT switch (S3) with pins 1 through 6. Pin 6 is connected to the +3V3_MCU supply. Pin 3 is connected to the GPIO32 pin (J2_18) through a 10.0k resistor (R16). Pin 2 is connected to the GPIO024 pin (J1_8) through a 10.0k resistor (R15). Pin 4 is connected to the GND. Pin 5 is connected to GND. Pin 1 is connected to GND. The switch is controlled by a signal from the MCU.

Selected Boot Mode Chart

Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

EQEP Routing

The diagram illustrates the routing for two SN74LV4053APWR multiplexers (U5 and U7) and a 2-to-1 multiplexer (S5).

U5 (SN74LV4053APWR) Connections:

- VCC:** +3V3_MCU (Pin 16)
- INH:** 6
- 1-COM:** 14 (GPIO14)
- 2-COM:** 15 (GPIO33)
- 3-COM:** 4 (GPIO26)
- GND:** 8
- Outputs:**
 - 1Y0 (12): GPIO14_Q2A
 - 1Y1 (13): GPIO14_BP - J2_17
 - 2Y0 (2): GPIO33_Q2B
 - 2Y1 (1): GPIO33_BP - J2_11
 - 3Y0 (5): GPIO26_Q2I
 - 3Y1 (3): GPIO26_BP - J2_12

U7 (SN74LV4053APWR) Connections:

- VCC:** +3V3_MCU (Pin 16)
- INH:** 6
- 1-COM:** 14 (GPIO20)
- 2-COM:** 15 (GPIO21)
- 3-COM:** 4 (GPIO43)
- GND:** 8
- Outputs:**
 - 1Y0 (12): GPIO20_Q1A
 - 1Y1 (13): GPIO20_BP - J6_57
 - 2Y0 (2): GPIO21_Q1B
 - 2Y1 (1): GPIO21_BP - J2_32
 - 3Y0 (5): GPIO43_Q1I
 - 3Y1 (3): GPIO43_BP - J6_52

S5 (2-to-1 Multiplexer) Connections:

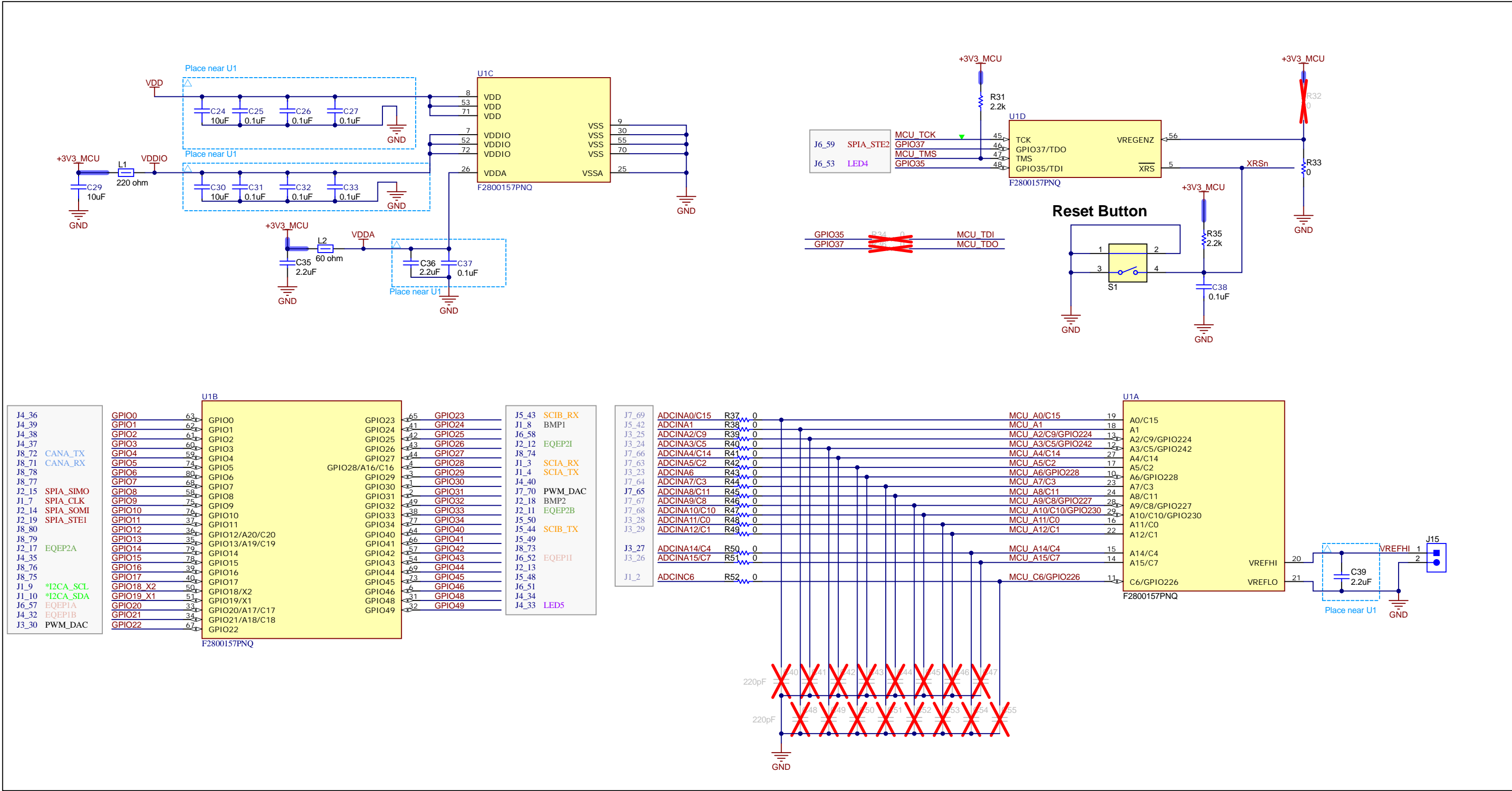
- Inputs:**
 - 6: BP (from U5 1Y0)
 - 3: BP (from U7 1Y0)
- Outputs:**
 - 5: QEP1_SEL
 - 2: QEP2_SEL
- Control:**
 - 4: J12
 - 1: J13
- GND:** 8

Legend:

- S5 (1, UP): QEP signals are routed to the BoosterPac k Headers (default)
- S5 (0, DOWN): QEP signals are routed to the QEP Headers

The diagram illustrates a PWM DAC circuit. It features two op-amp comparators, U18A and U18B. U18A's non-inverting input (pin 1) is connected to a 3V3 MCU supply through resistor R78. Its inverting input (pin 3) is connected to a 3V3 MCU supply through resistor R83. U18A's output (pin 6) is connected to the 3V3 MCU supply through resistor R21. U18B's non-inverting input (pin 2) is connected to a 3V3 MCU supply through resistor R23. Its inverting input (pin 4) is connected to a 3V3 MCU supply through resistor R21. The outputs of U18A and U18B are connected to the 3V3 MCU supply through capacitors C13 and C14, respectively. The 3V3 MCU supply is also connected to the 3V3 MCU pin through capacitor C15. The circuit is powered by a 3V3 MCU supply and a GND connection.

[illegible]



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A

B

C

D

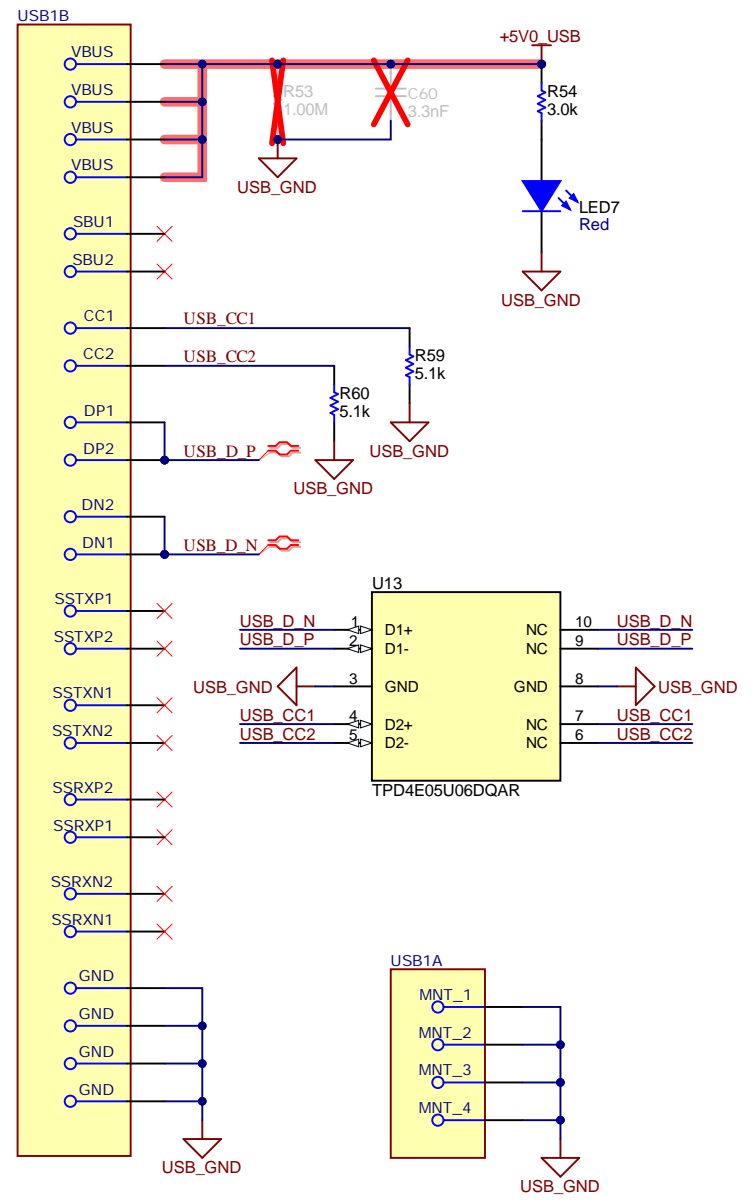
A

B

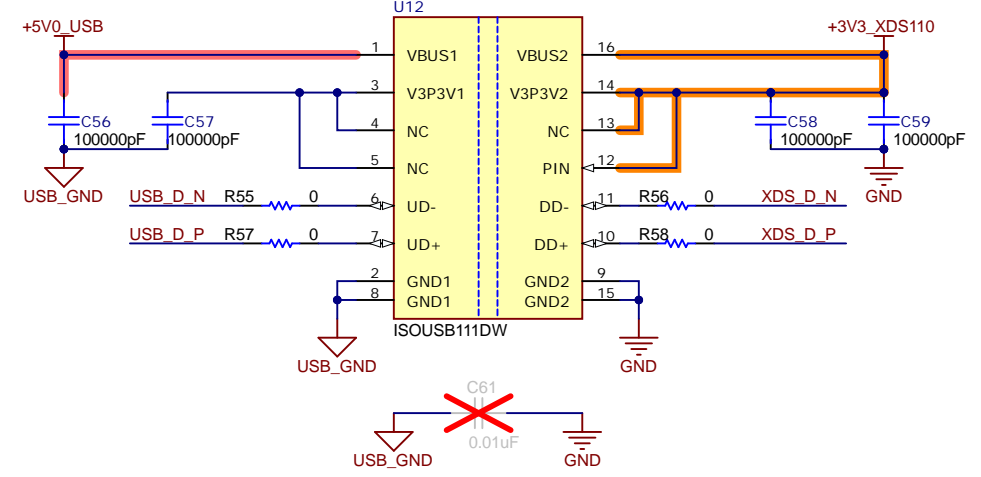
C

D

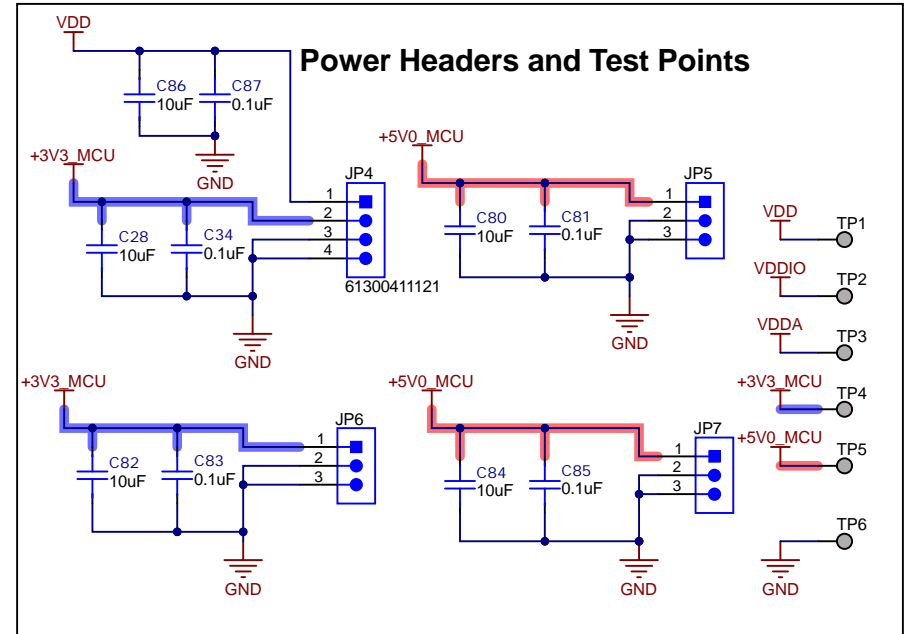
USB-C Connector



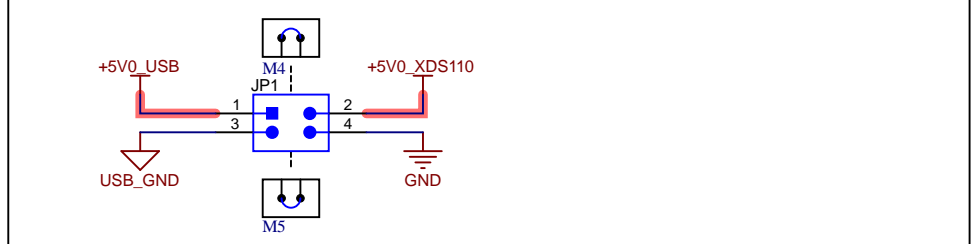
USB Isolation



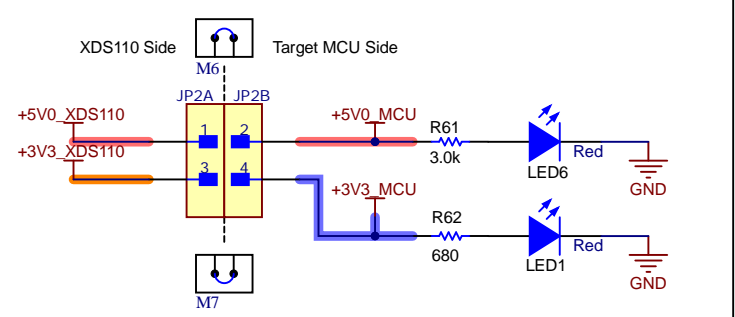
Power Headers and Test Points



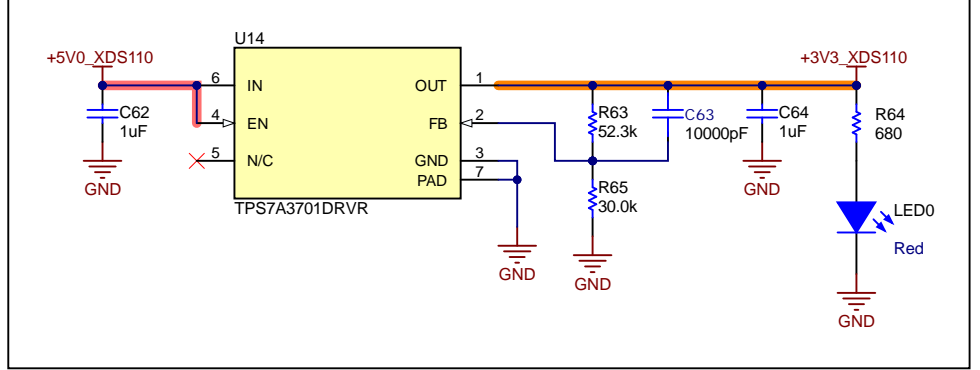
PWR & GND Isolation Boundary



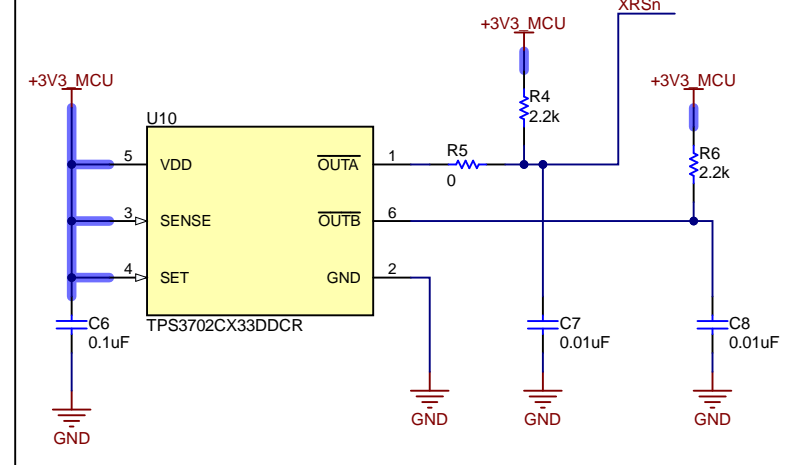
5V & 3.3V Isolation Boundary



5V to 3.3V

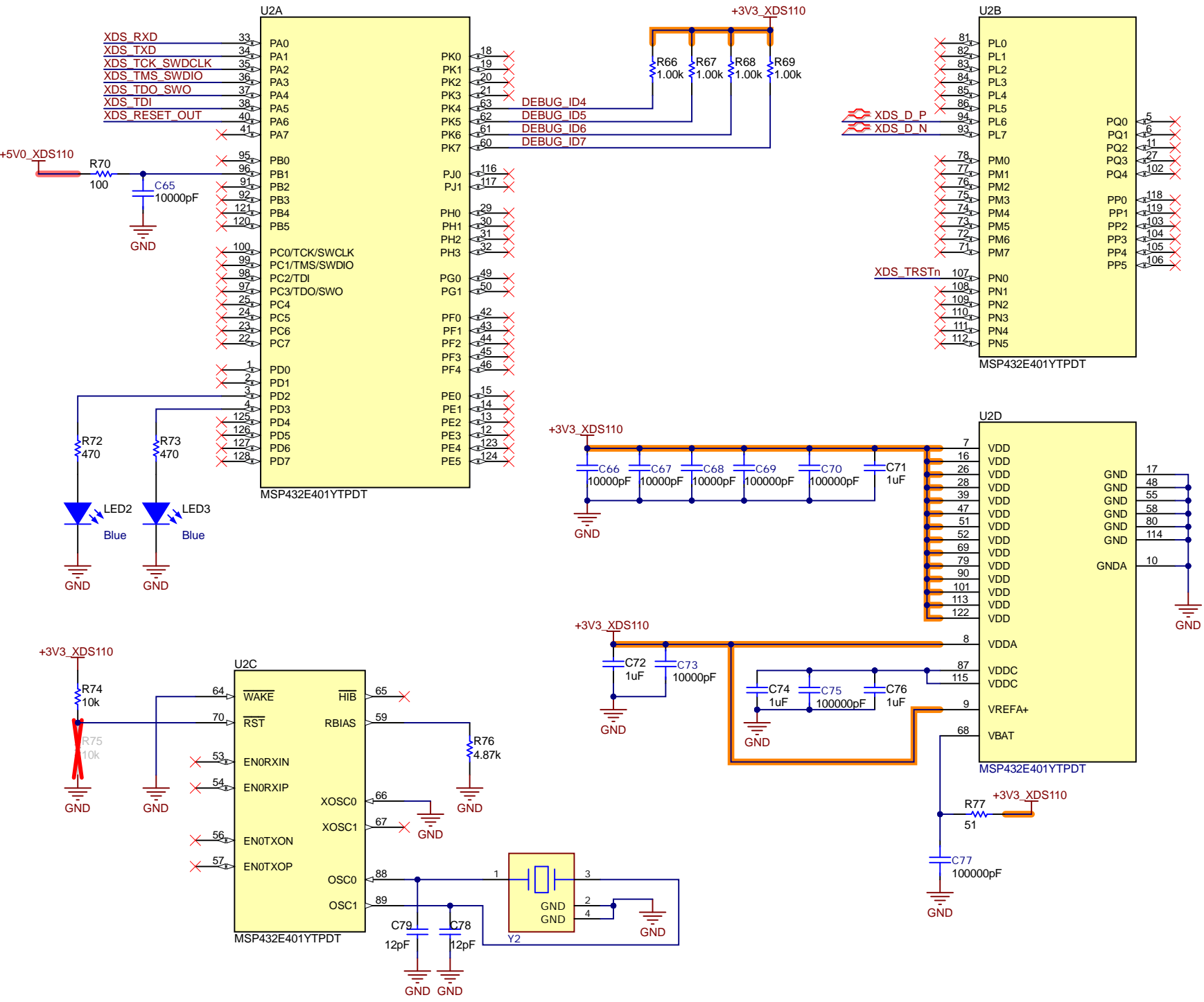


System Supervisory Circuit

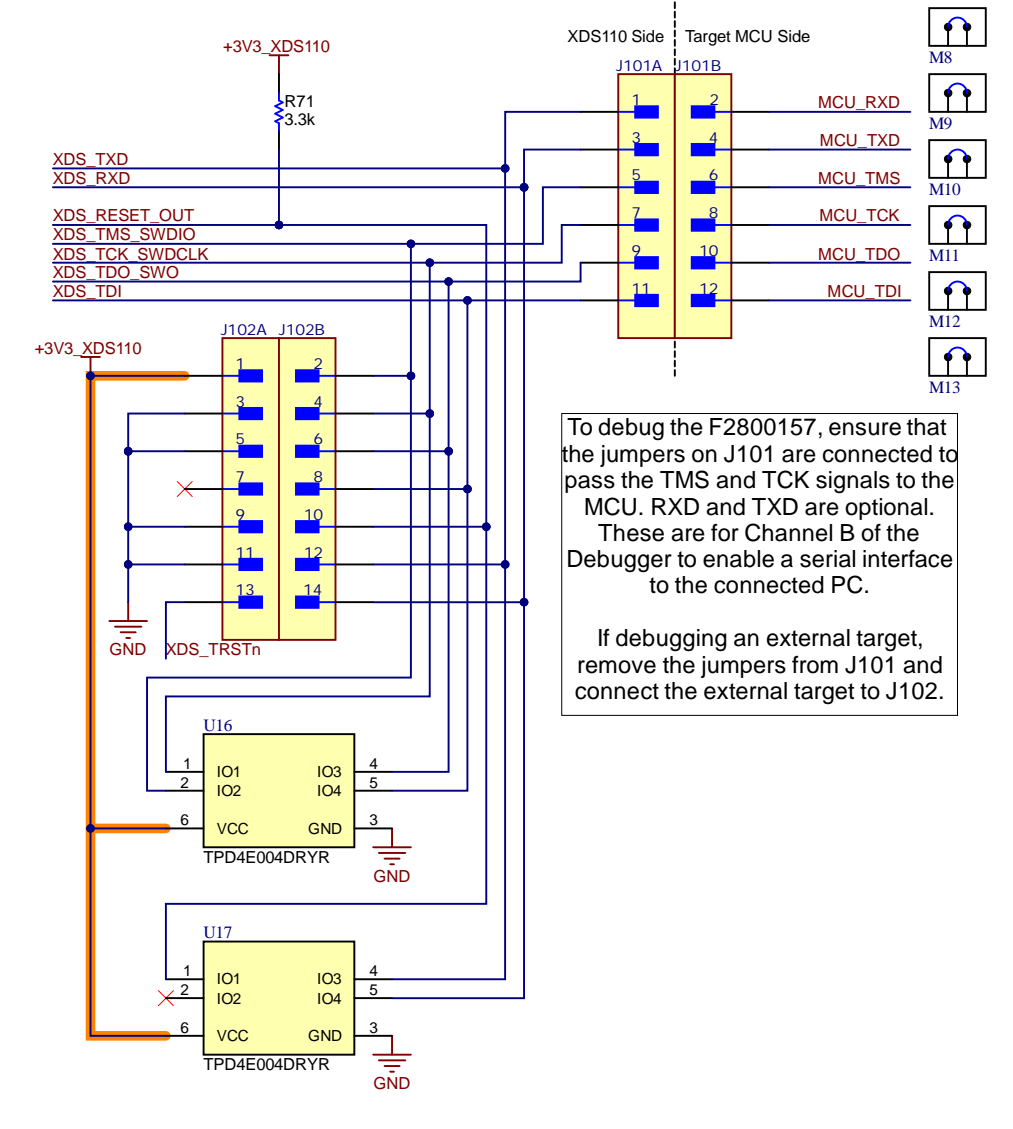


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XDS110 Device



XDS110 Target Interface



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A

B

C

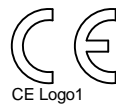
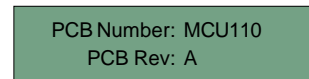
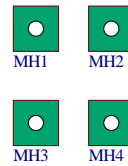
D

A

B

C

D



ZZ1

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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TID #:		Project Title: LAUNCHXL-F2800157				
Number: MCU110		Rev: A		Sheet Title:		
SVN Rev:		Assembly Variant: 001		Sheet: 7 of 7		
Drawn By:		File: MCU110A_Hardware.SchDoc		Size: B		
Engineer: Peter Luong		Contact: http://www.ti.com/support				