

AM62x STARTER KIT EVM

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REV	A
VER	0.04

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	14 OCT 2022	Drafted from E3A Schematics. Added Testpoint to TEMP_DIODE_P pin of SoC. Changed the GPIO_OLDI_RSTn net name to GPIO_TS_RSTn.Changed the DDR4 part from MT40A1G16KD-062E IT:E to MT40A1G16TB-062E IT:F. Changed the eMMC part from MTFC16GAPALBH-IT to MTFC32GAZAQHD-IT. Added the second GPIO Expander U110 Part# TCA6408ARGTR. Changed the part SN74AVC4T245RSVR to SN74AVC4T245DGVR.Changed the I2C buffer parts to TCA9517DR.	Mistral Design Team		
0.02	16 OCT 2022	Removed Wilink module and added M.2 connector	Mistral Design Team		
0.03	23 NOV 2022	Added 2x 47uF on VCC_5V0. DNI'd C432, C433(10uF) and changed C415 to 4.7uF. Added 22pF CAP across R108	Mistral Design Team		
0.04	1 Dec 2022	Removed MMC2 connector section (J18) and associated resistors	Mistral Design Team		

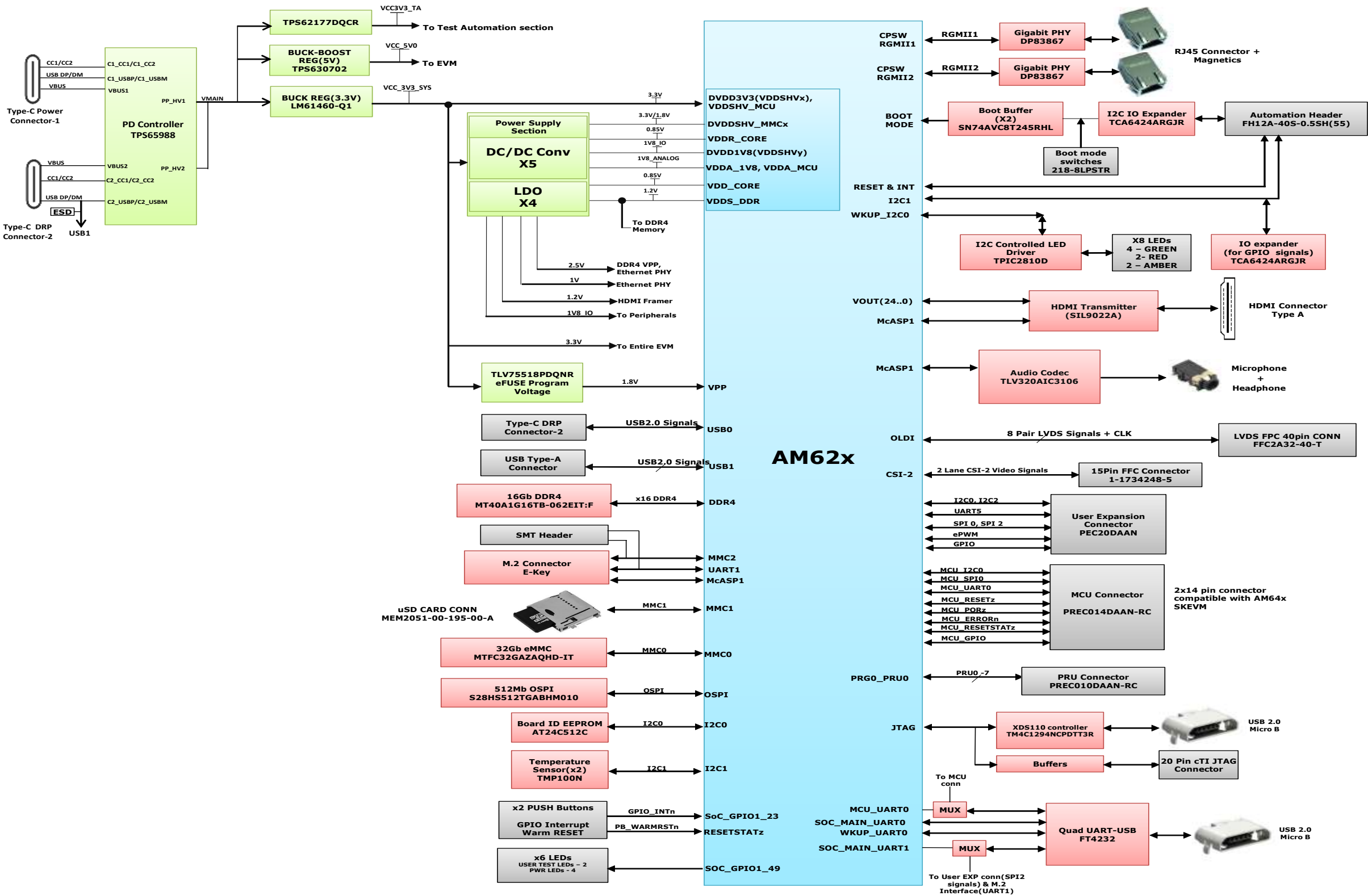
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BLOCK DIAGRAM AM62x SKEVM

Main Block Diagram



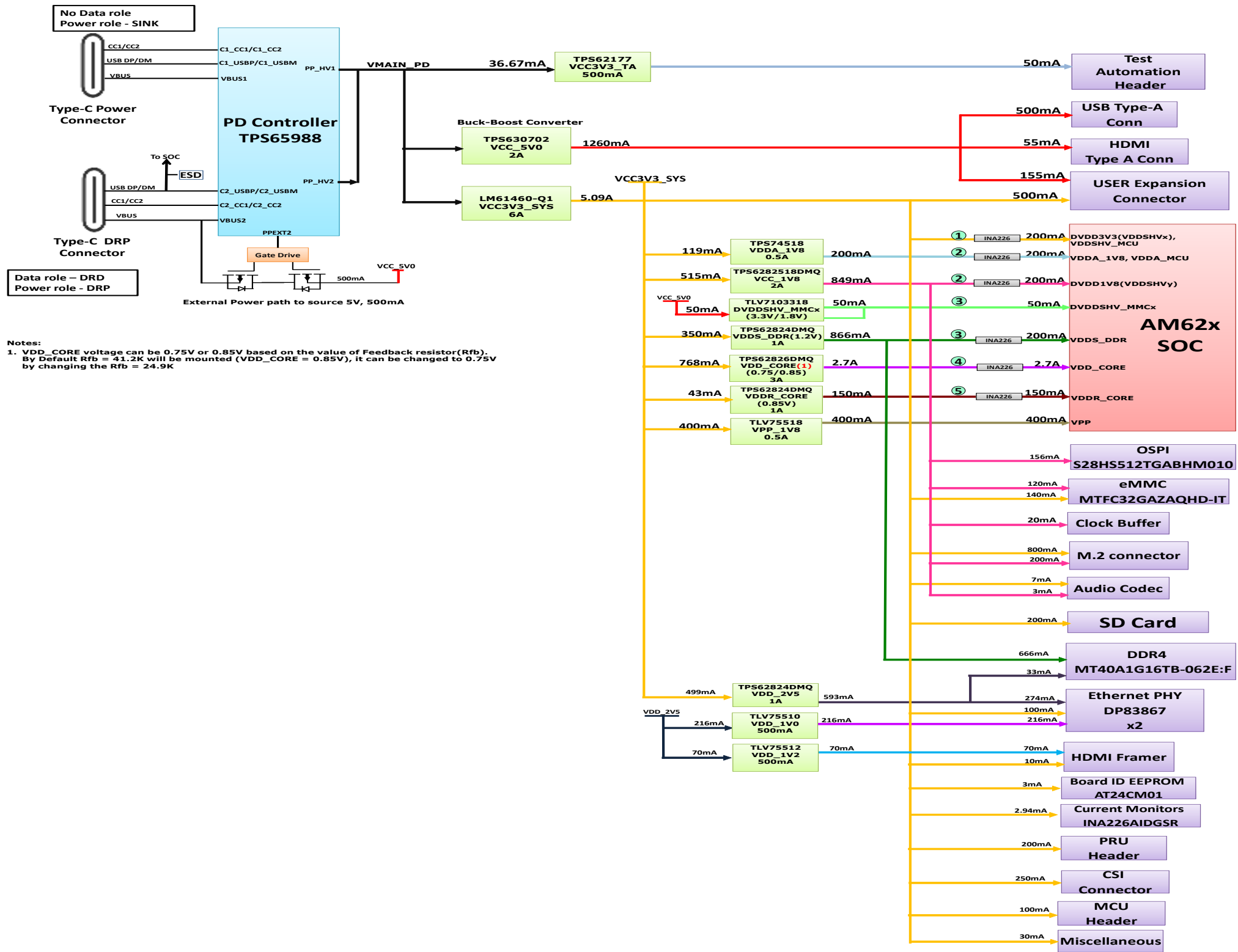
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Title BLOCK DIAGRAM AM62x SKEVM

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POWER BLOCK DIAGRAM



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Title POWER BLOCK DIAGRAM

Size PROC114A(002)

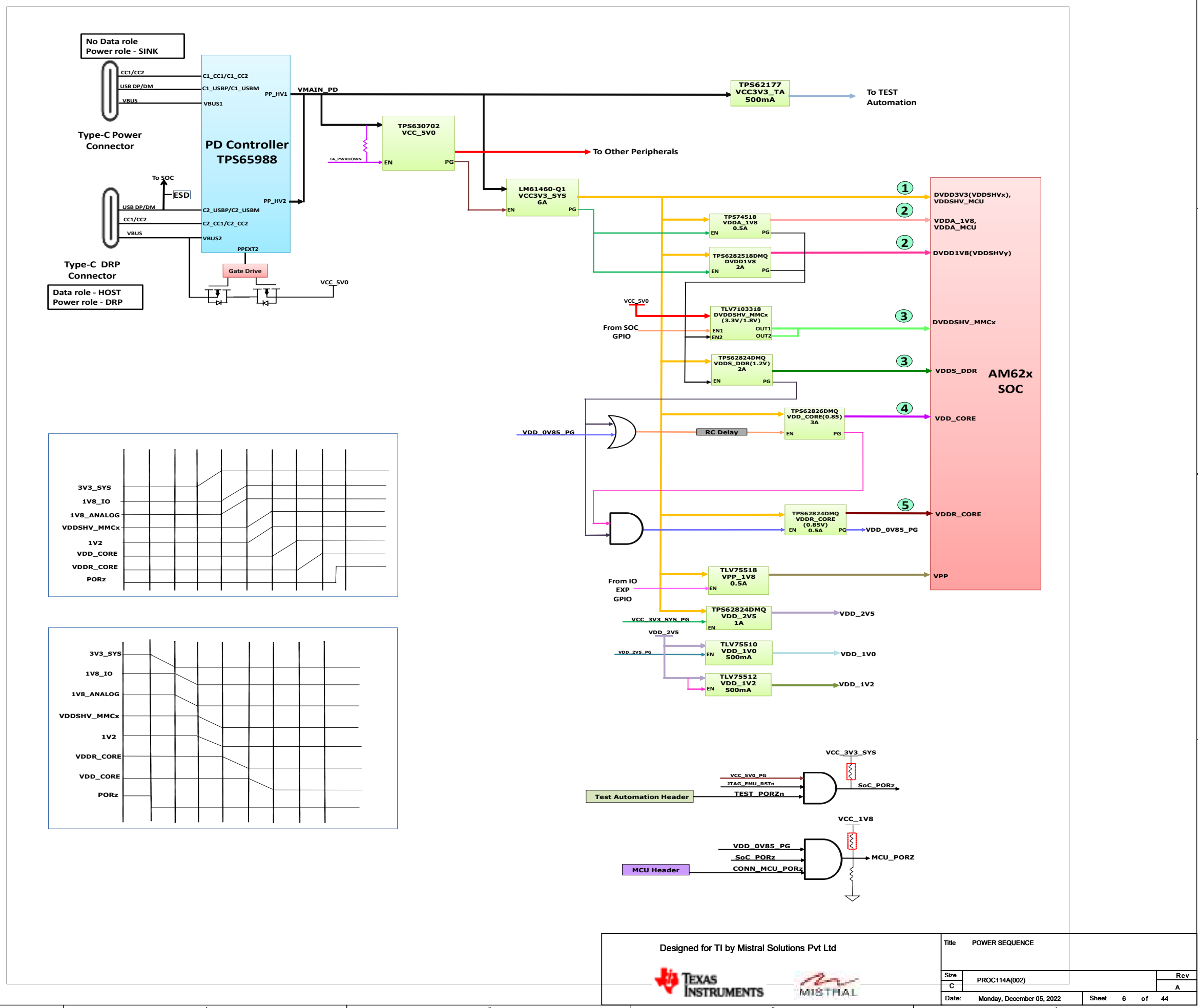
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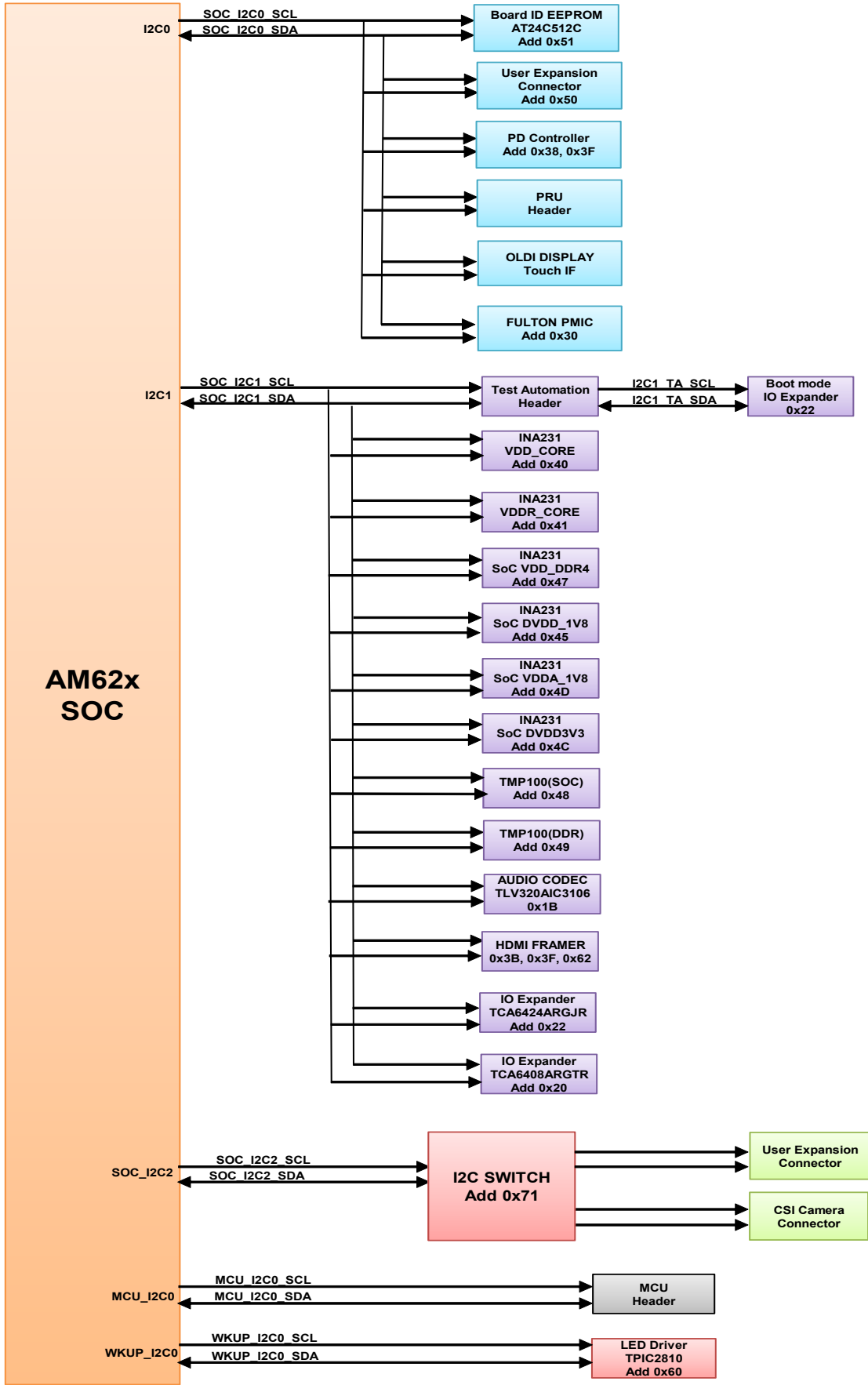
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POWER SEQUENCE



I2C TREE



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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPIO_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
	PRU Connector Interrupt									
	PMIC_INTn									
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER – P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER – P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 02										
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER – P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER – P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER – P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER – P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

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Title GPIO MAPPING TABLE

Size

PROC114A(002)

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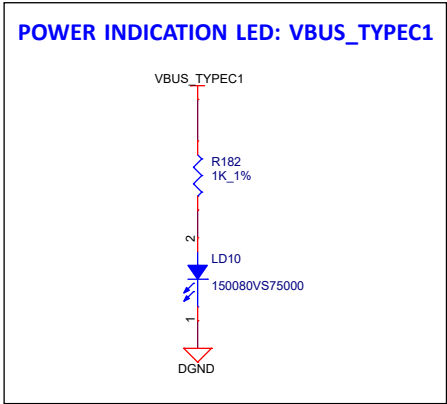
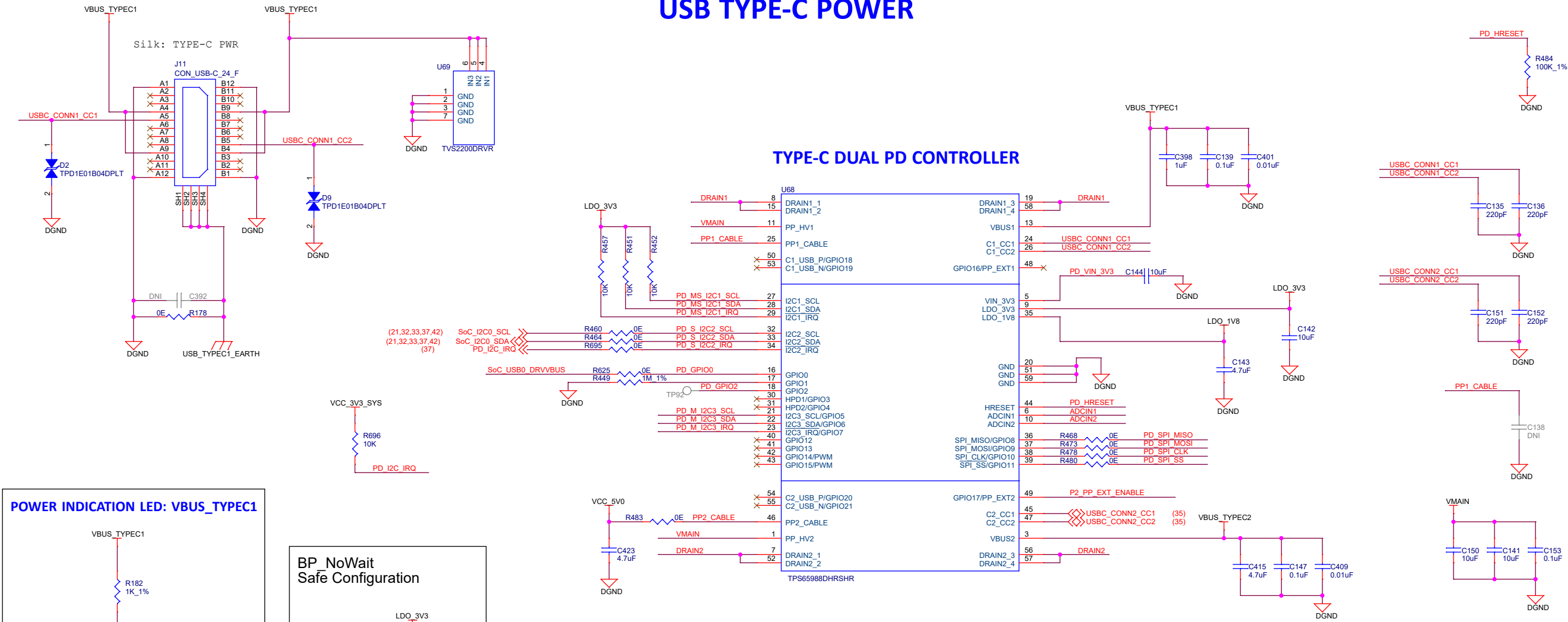
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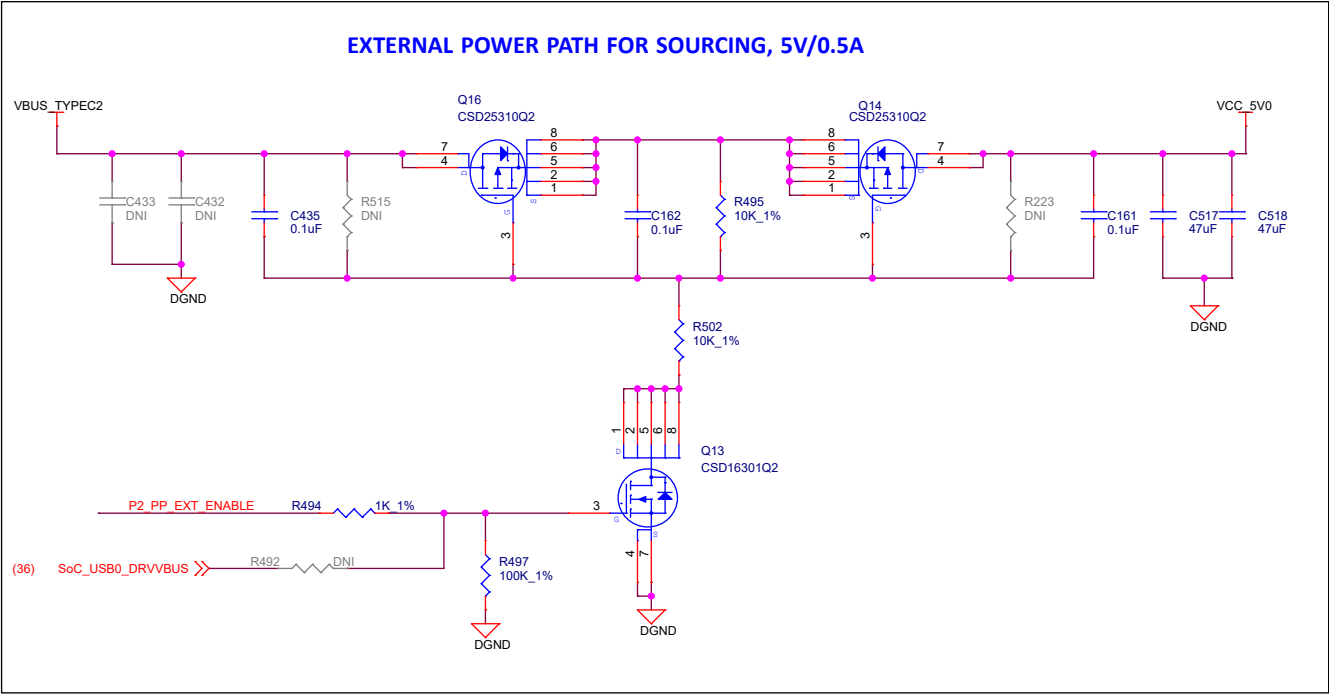
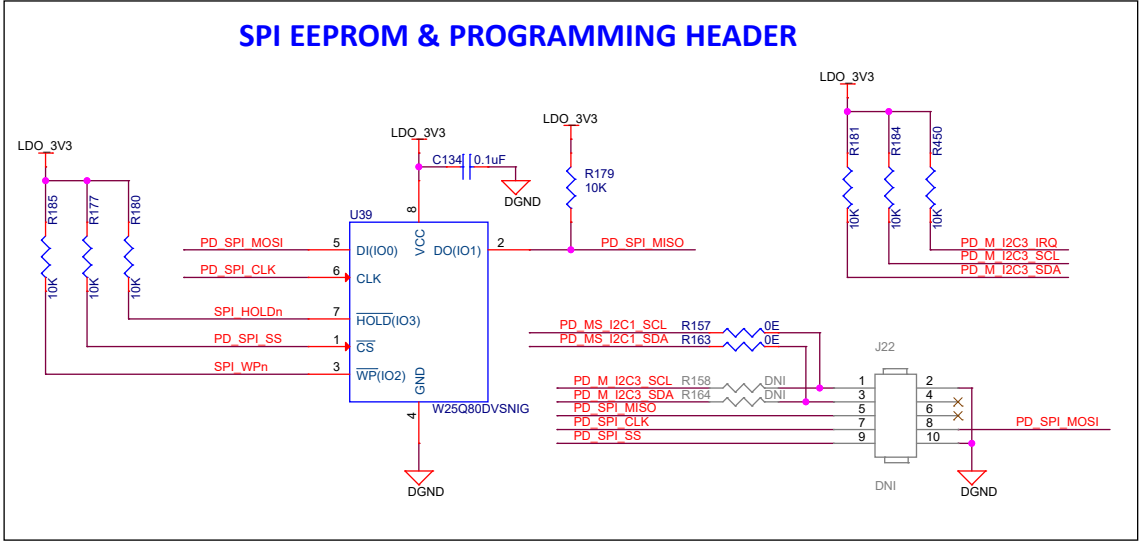
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USB TYPE-C POWER



I2C Slave Address	Port1	Port2
I2C2 (Default)	0x38	0x3F
I2C1	0x20	0x24

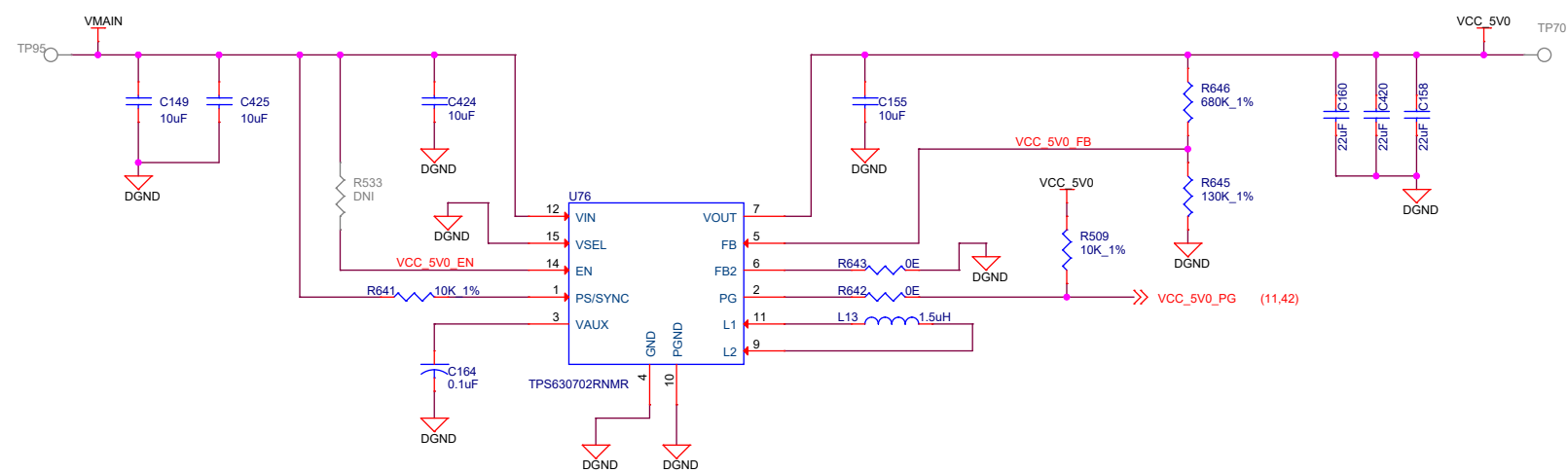


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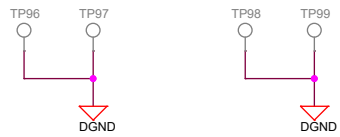
PERIPHERAL POWER SUPPLY-1



Power Cycle control from Test Automation



GROUND TEST POINTS



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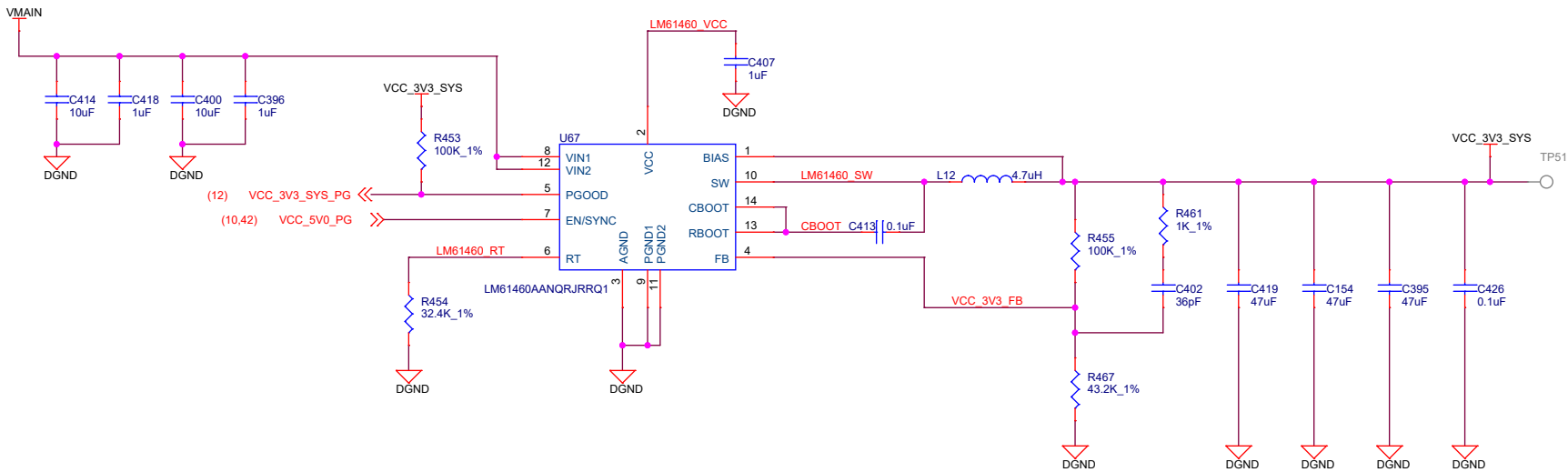


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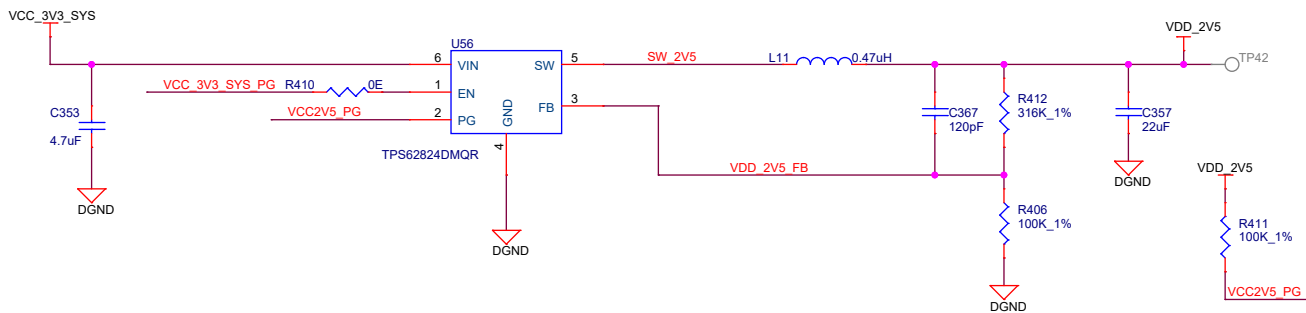
PERIPHERAL POWER SUPPLY-2

VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A

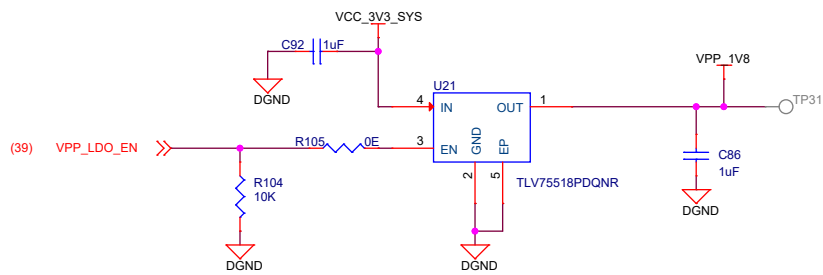
3.3V, 6.0AMPS SUPPLY



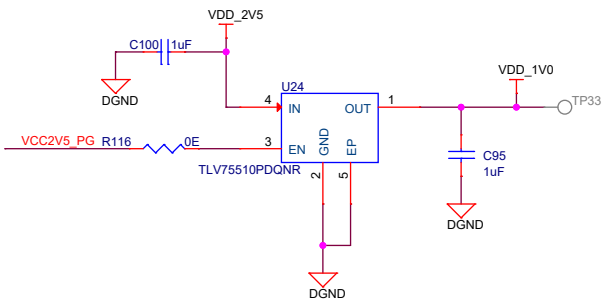
2.5V, 1.0AMPS SUPPLY



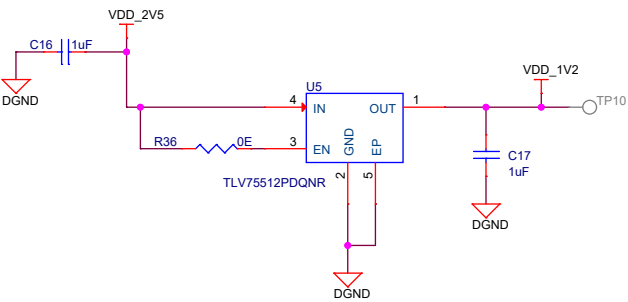
1.8V VPP, 0.5AMPS SUPPLY



1.0V, 0.5AMPS SUPPLY



1.2V, 0.5AMPS SUPPLY



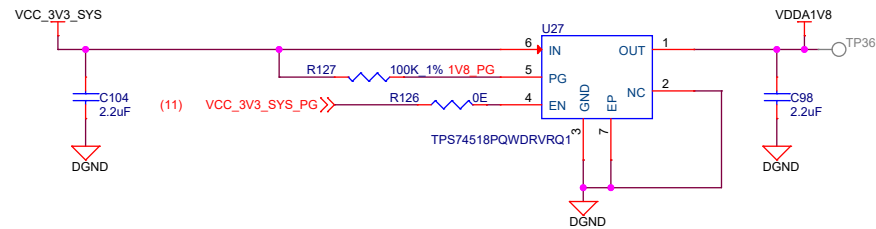
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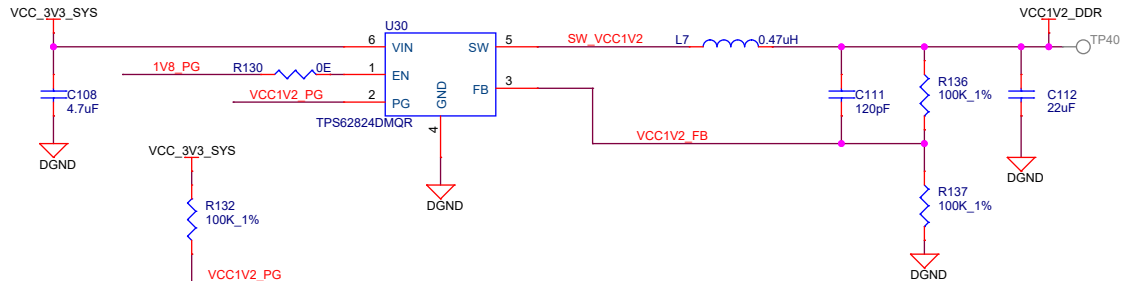
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SOC POWER SUPPLY

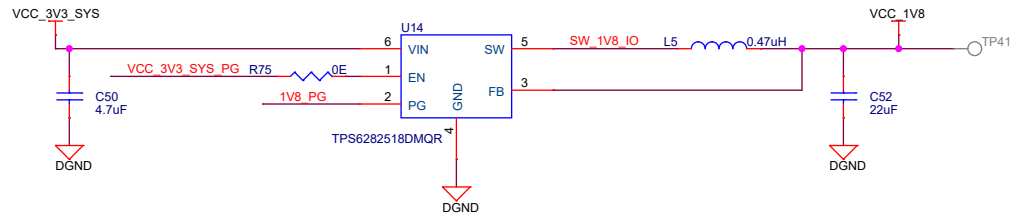
1.8V ANALOG, 0.5 AMPS SUPPLY



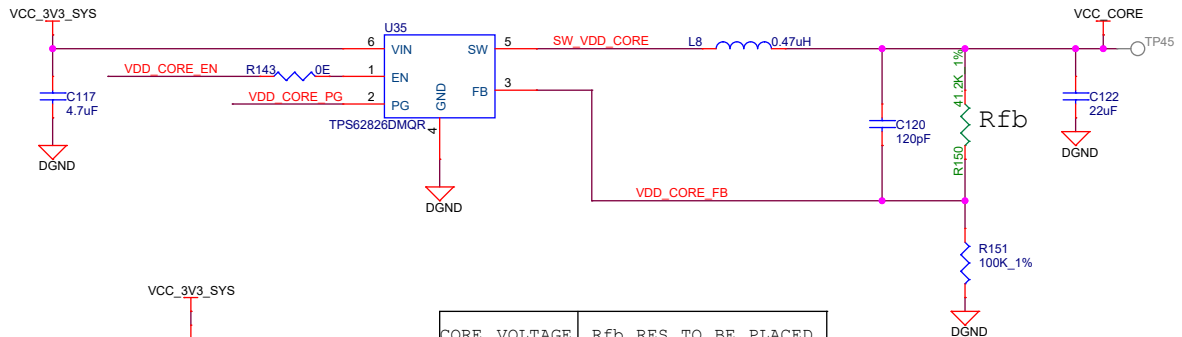
1.2V , 1.0 AMPS SUPPLY



1.8V IO, 2.0 AMPS SUPPLY

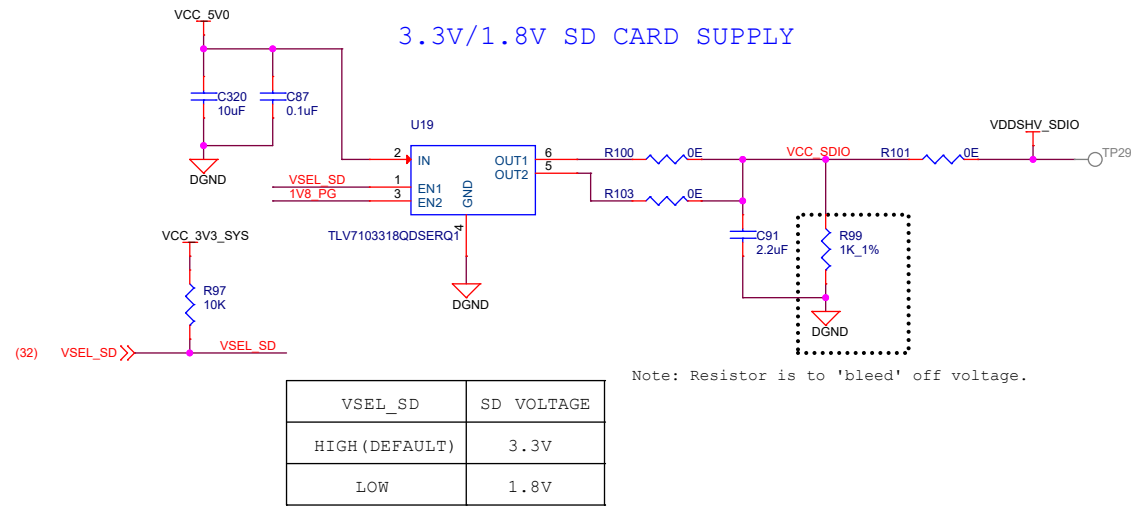


0.75V/0.85V , 3.0 AMPS SUPPLY



CORE VOLTAGE	Rfb RES TO BE PLACED
0.85V	Rfb = 41.2K
0.75V	Rfb = 24.9K

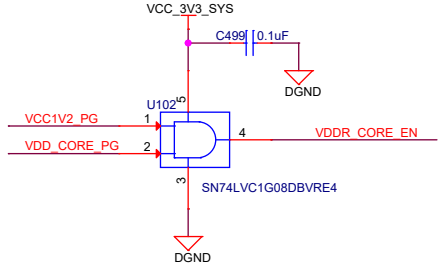
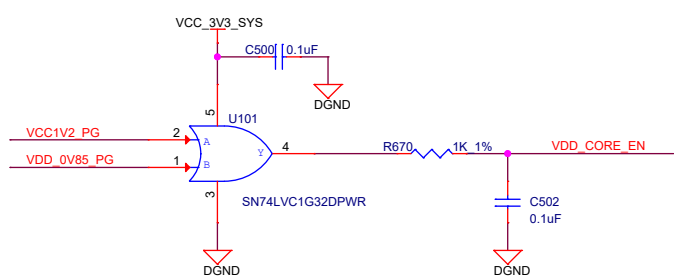
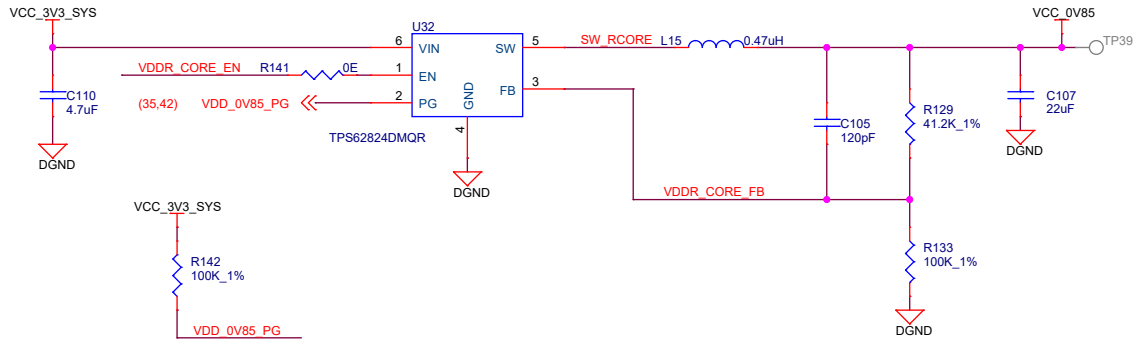
3.3V/1.8V SD CARD SUPPLY



VSEL_SD	SD VOLTAGE
HIGH (DEFAULT)	3.3V
LOW	1.8V

Note: Resistor is to 'bleed' off voltage.

0.85V, 0.5 AMPS SUPPLY



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Title SOC POWER SUPPLY

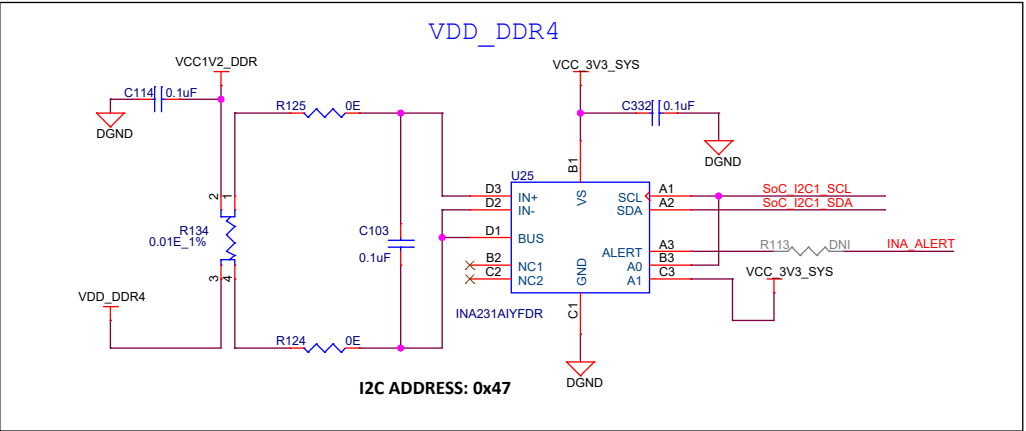
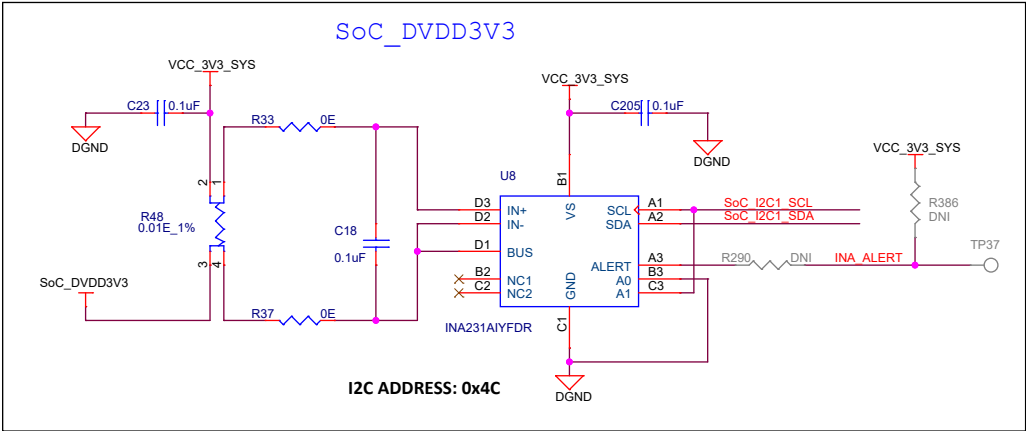
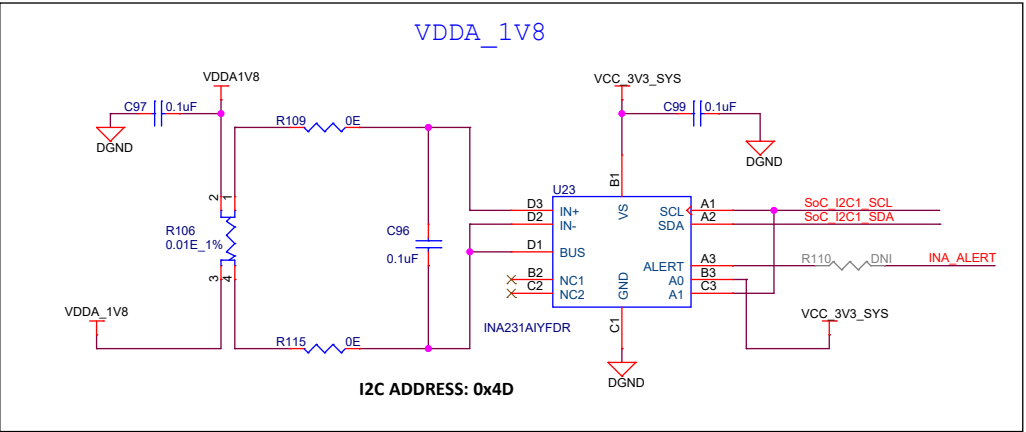
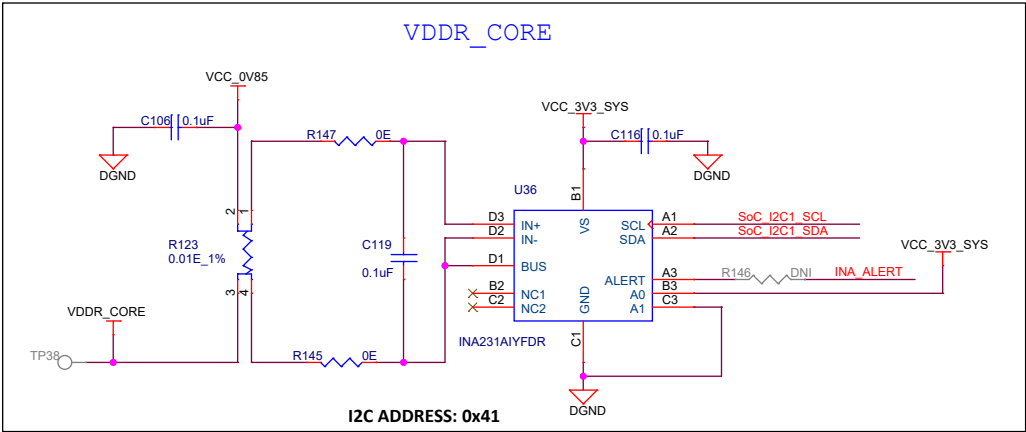
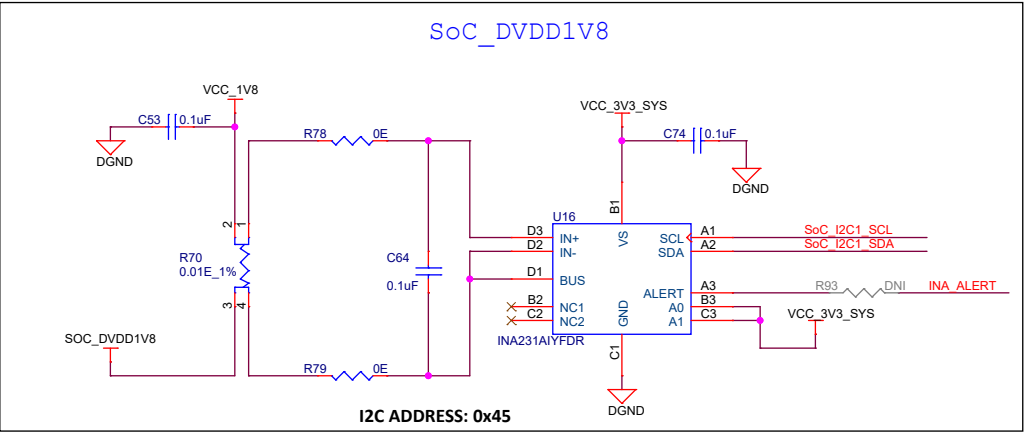
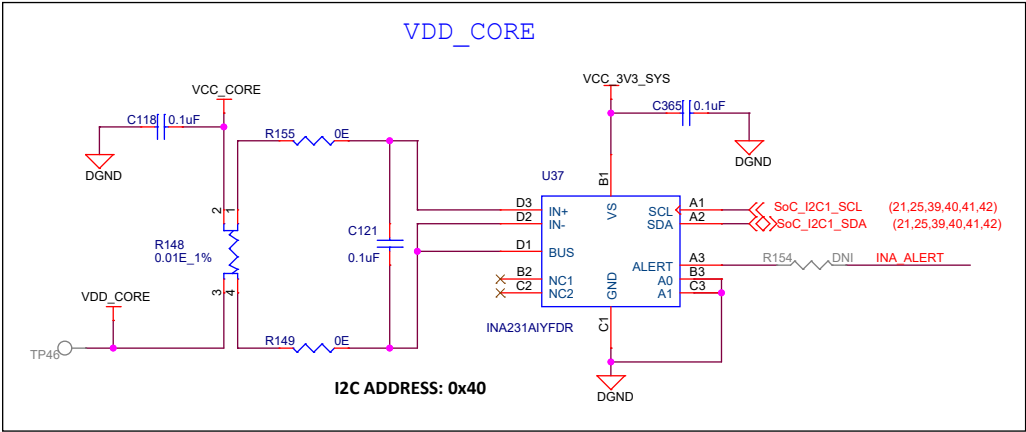
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CURRENT MONITORING DEVICES



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

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Title CURRENT MONITORING DEVICES

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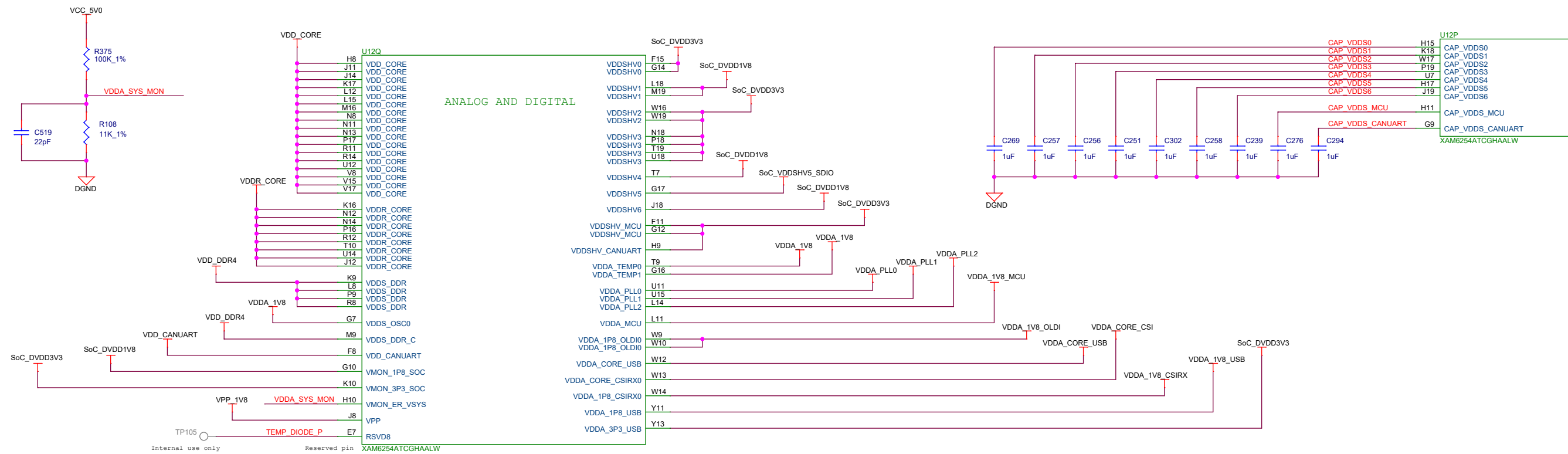
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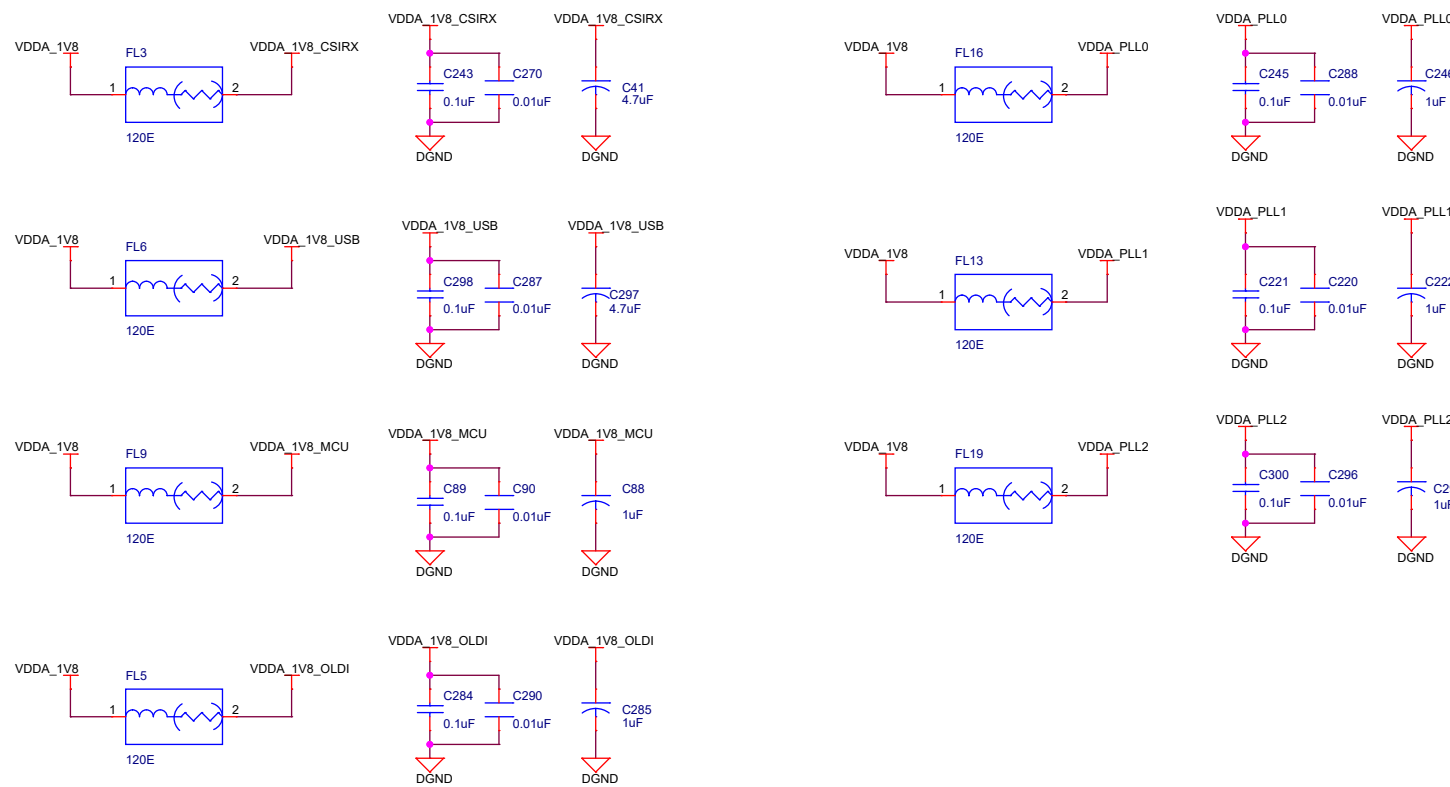
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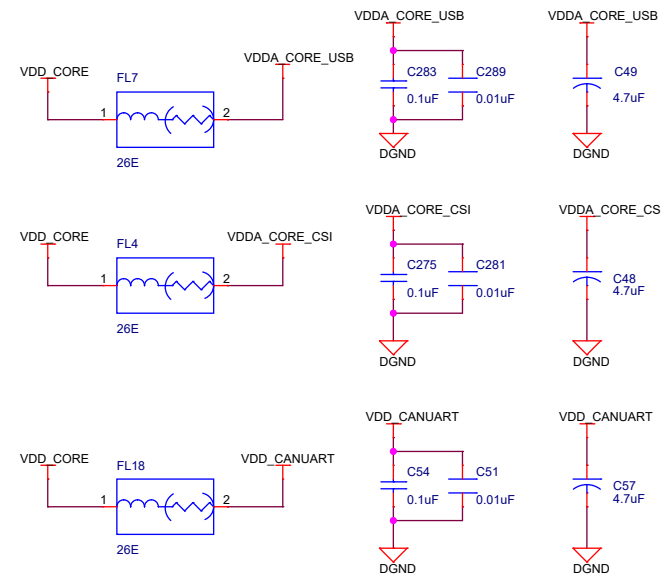
SOC POWER



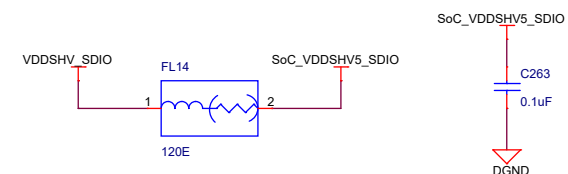
1.8V Analog SUPPLY



CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY

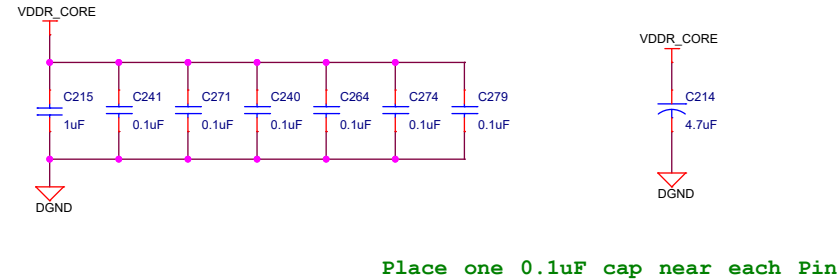
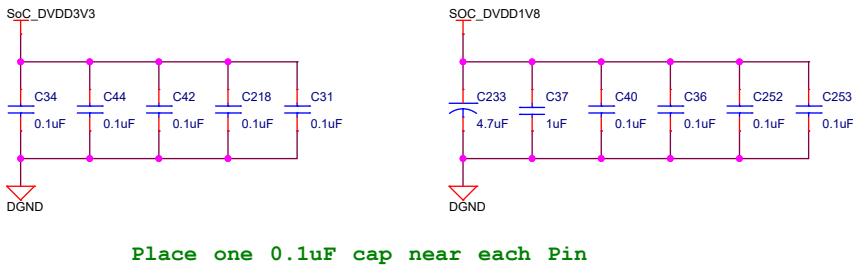
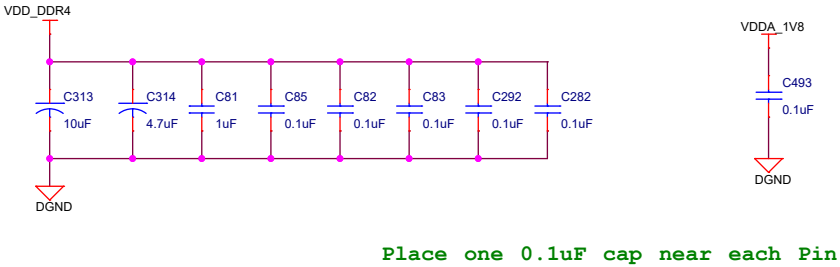
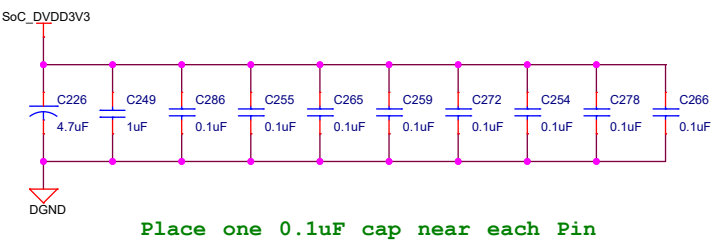
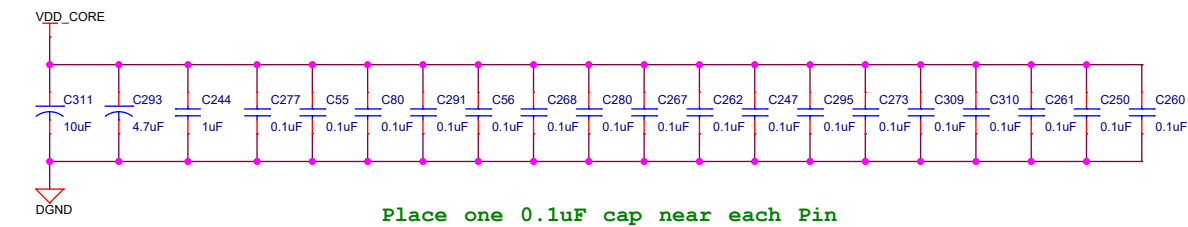


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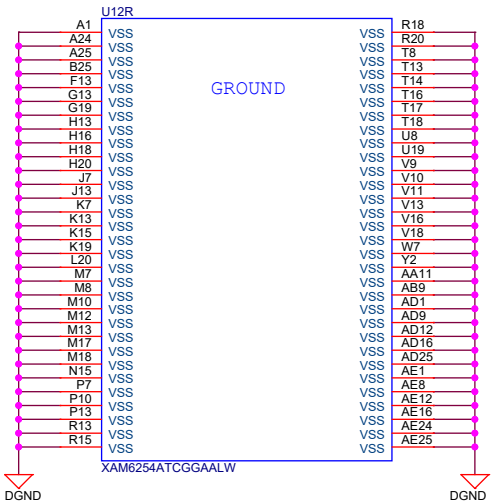


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SOC POWER DECAPS



SOC VSS



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Title SOC POWER CAPS & SOC VSS

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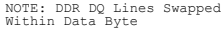
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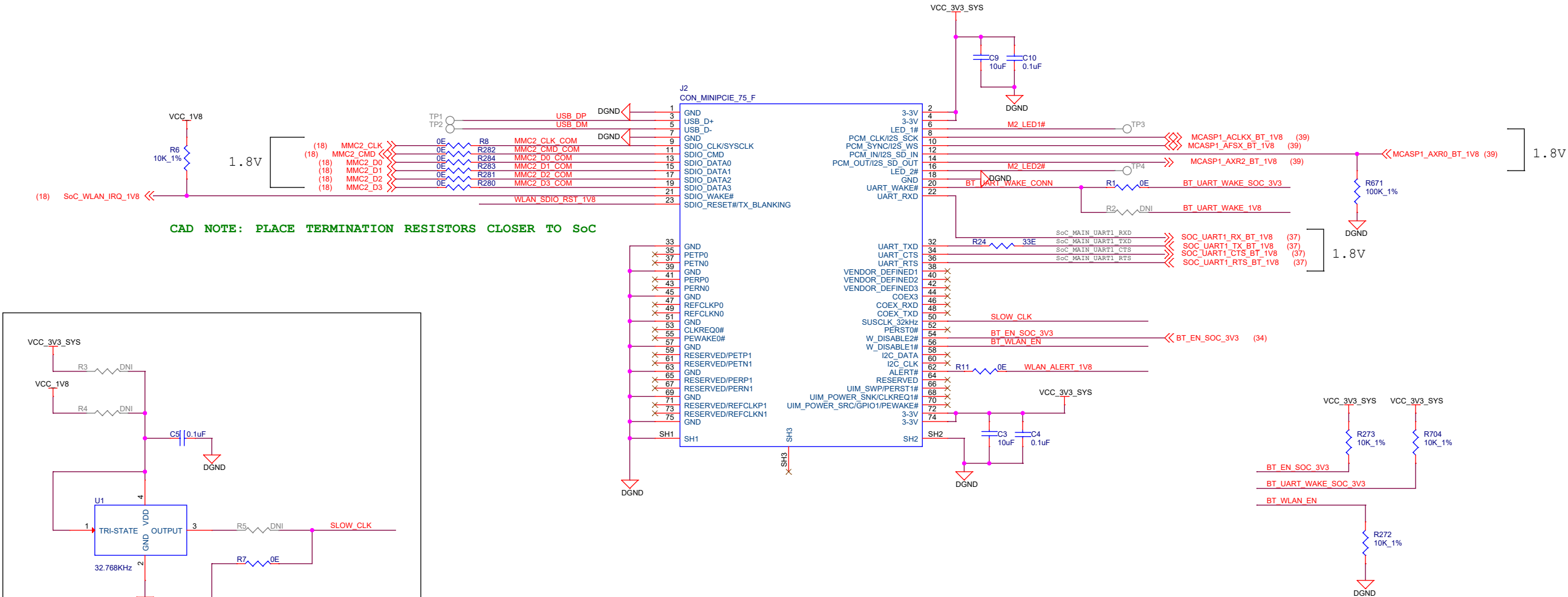


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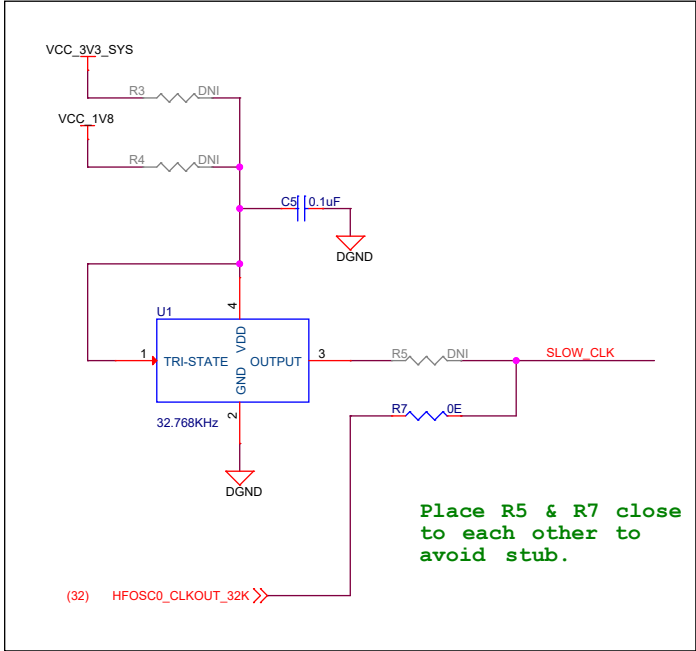
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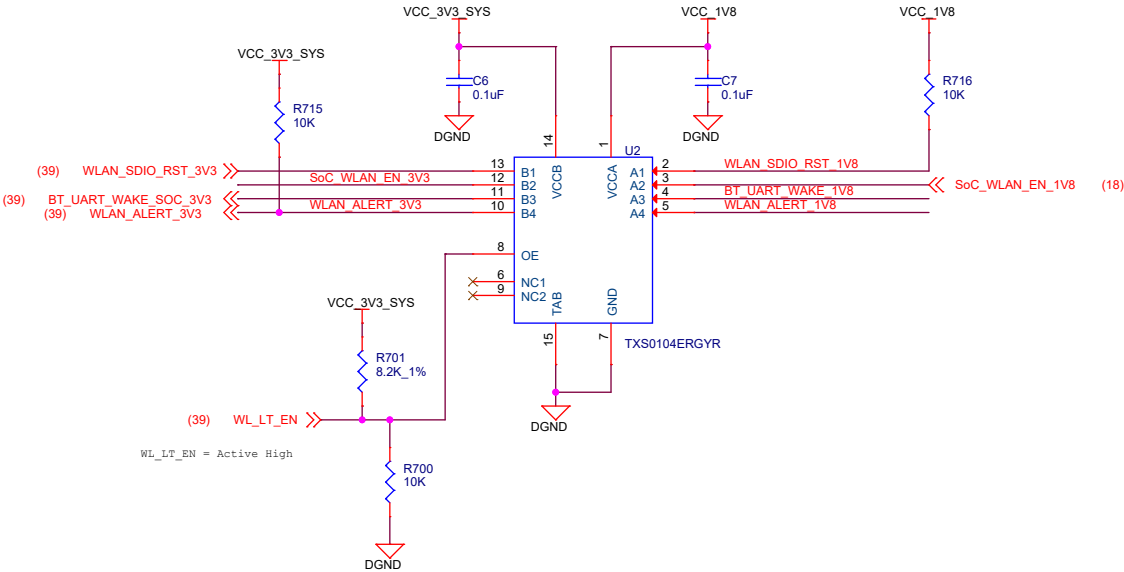
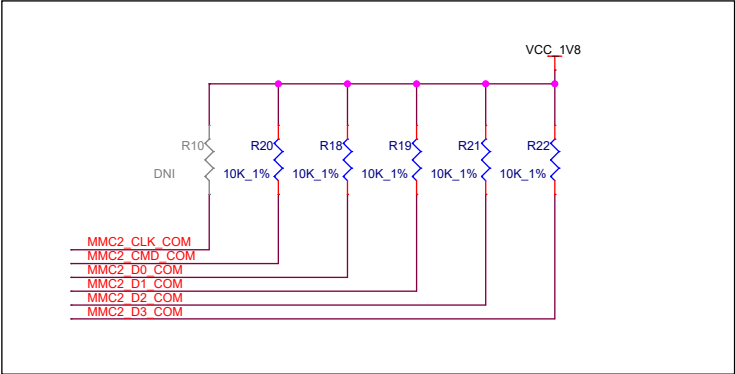
M.2 INTERFACE



CAD NOTE: PLACE TERMINATION RESISTORS CLOSER TO SoC



Place R5 & R7 close to each other to avoid stub.

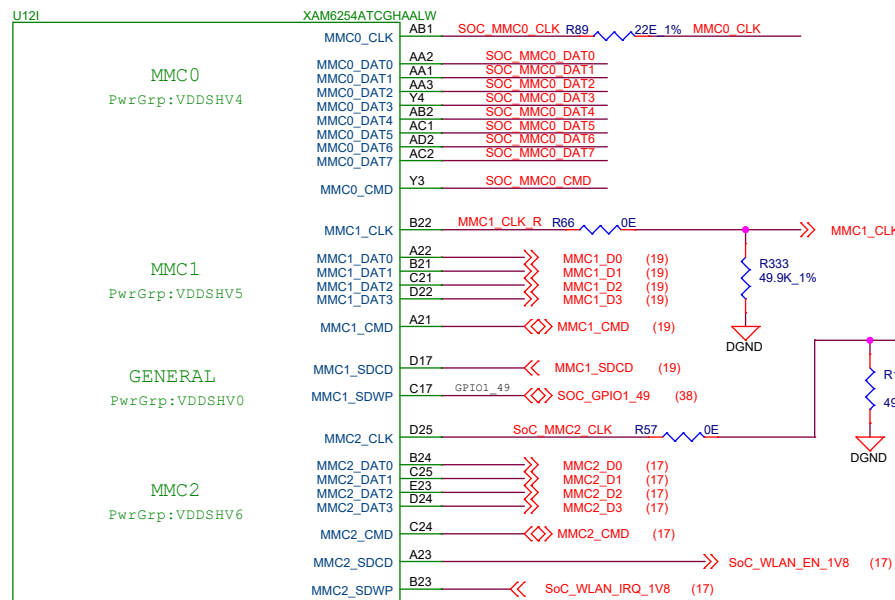


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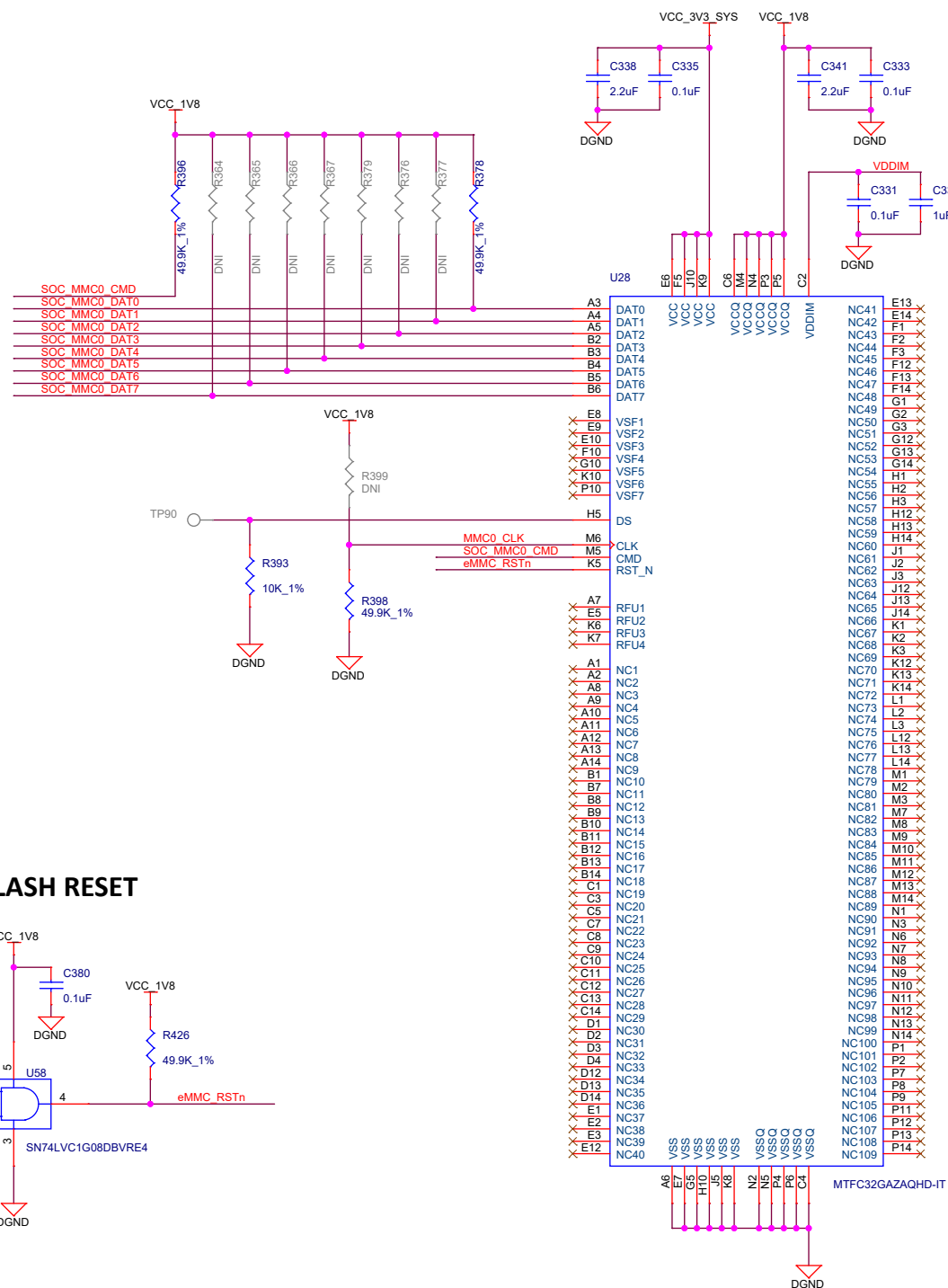


Title			WL1837 MODULE	
Size	PROC114A(002)		Rev	
C			A	
Date:	Monday, December 05, 2022	Sheet	17	of 44

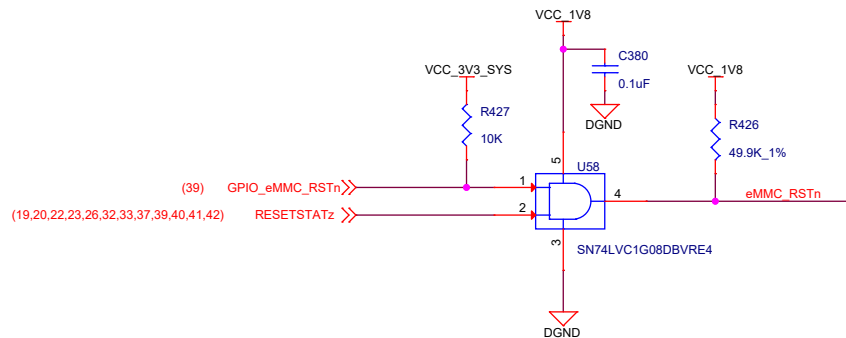
SOC - MMC Interface



eMMC FLASH



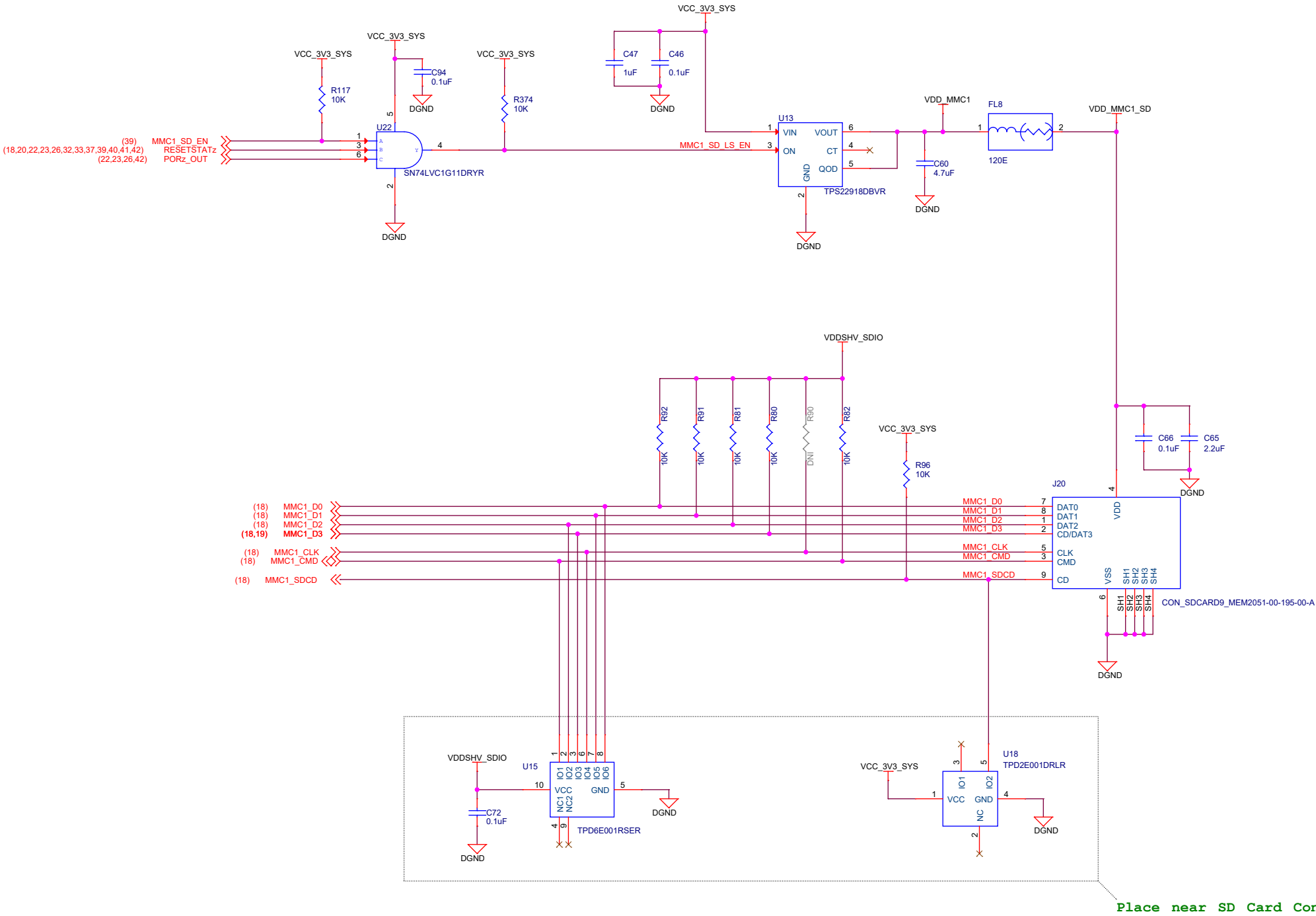
eMMC FLASH RESET



SD CARD INTERFACE

SD CARD RESET

LOAD SWITCH



Designed for T1 by Mistral Solutions Pvt Ltd



Title SD CARD INTERFACE

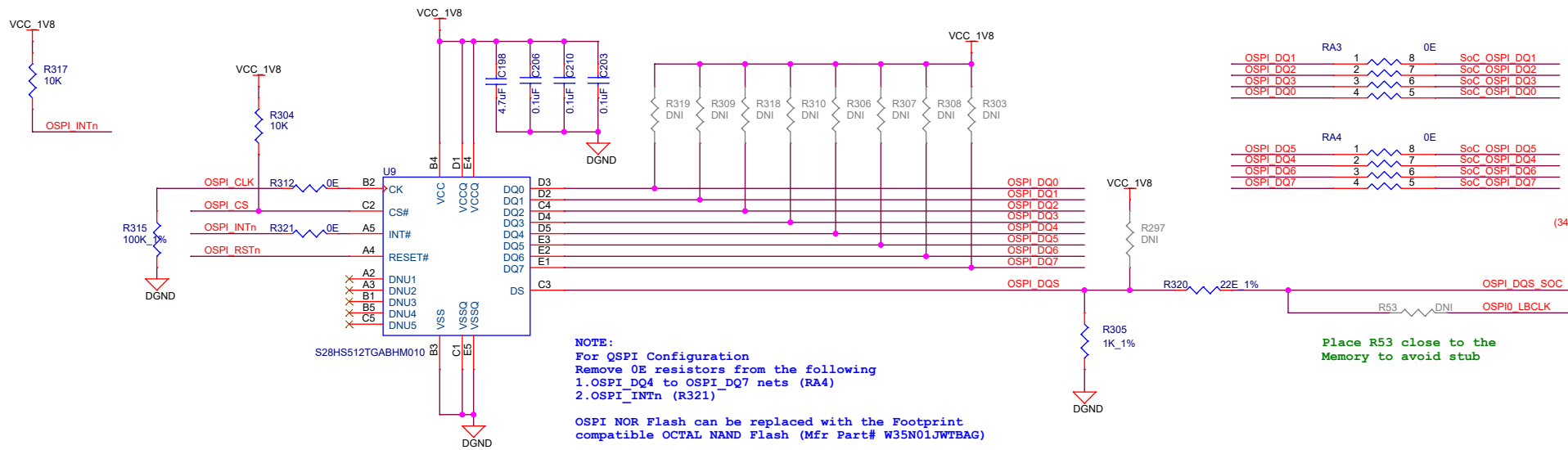
Size PROC114A(002)

Rev

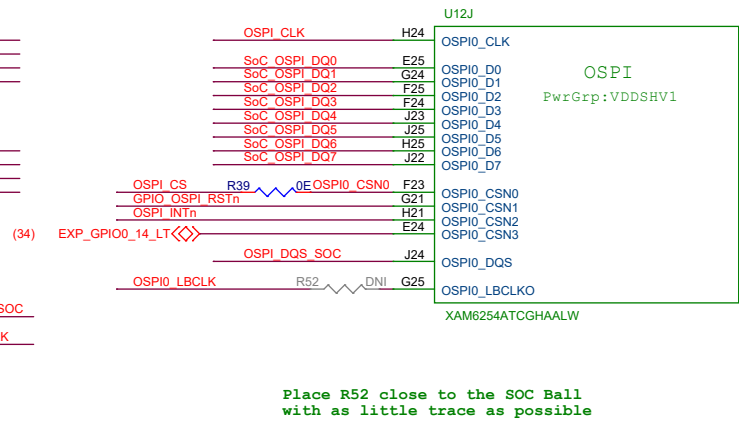
Date: Monday, December 05, 2022

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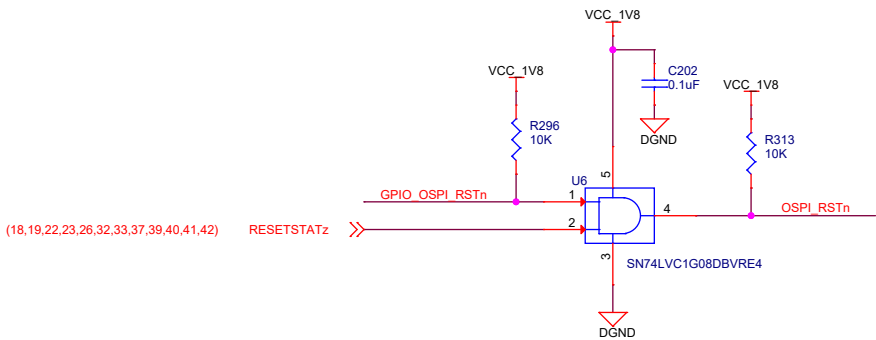
OSPI FLASH



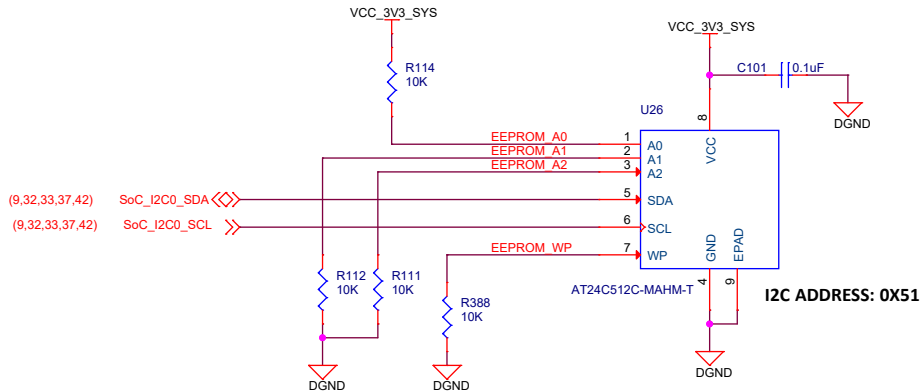
SOC OSPI INTERFACE



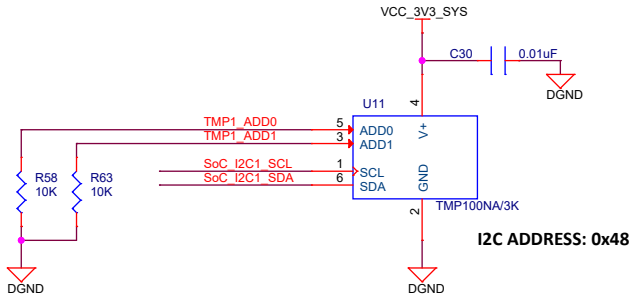
OSPI FLASH RESET



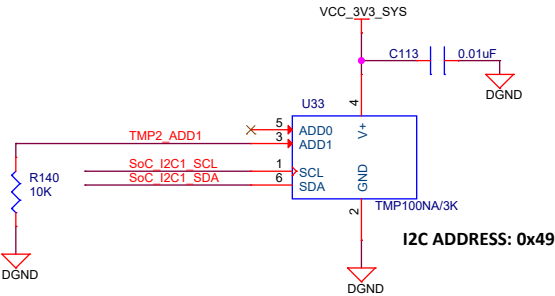
BOARD ID EEPROM



TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U11 CLOSE TO SoC



CAD NOTE: PLACE TEMP SENSOR U33 CLOSE TO DDR4



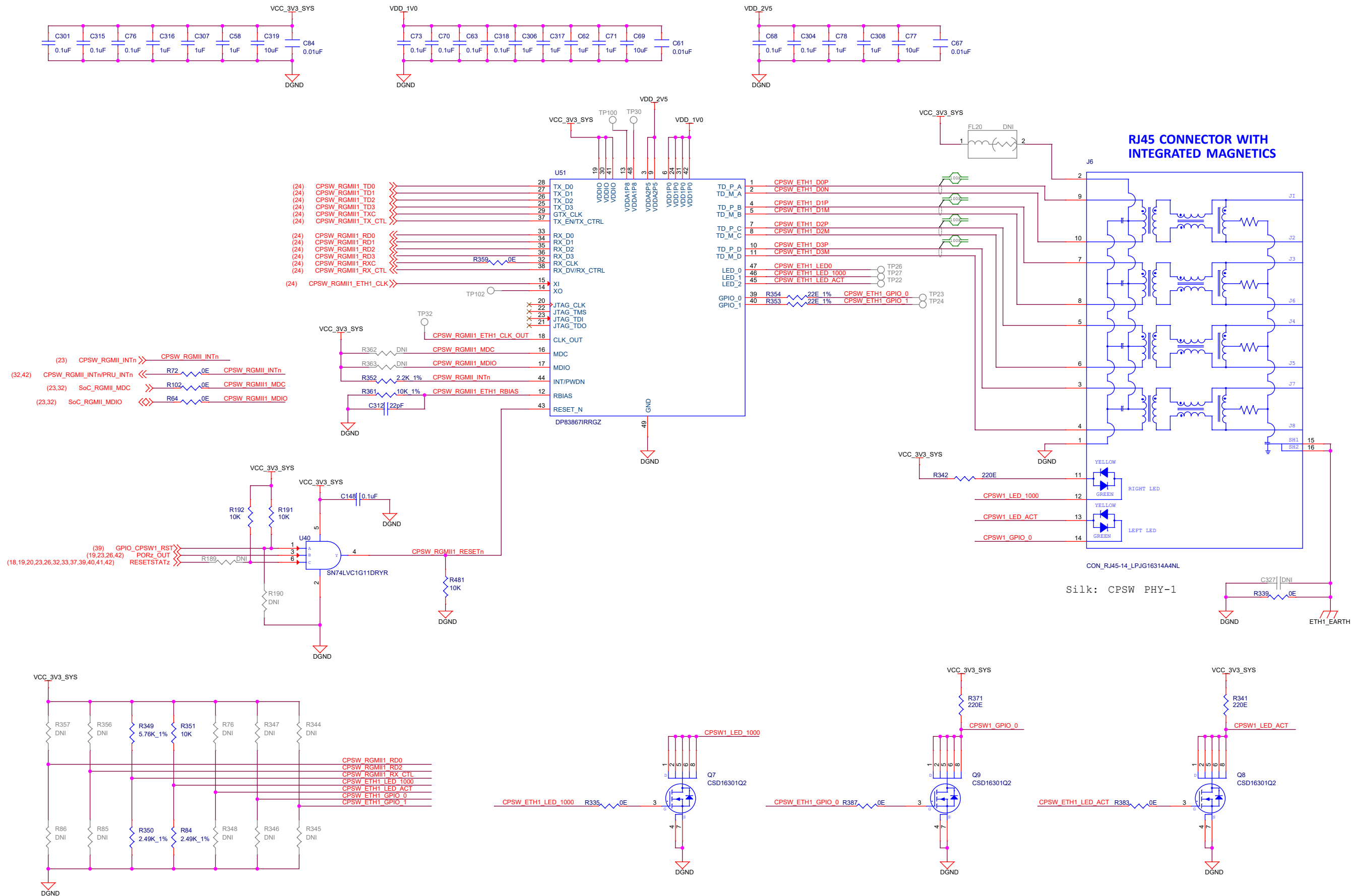
Designed for T1 by Mistral Solutions Pvt Ltd



Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size	PROC114A(002)	Rev
C		A
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CPSW RGMII 1 - PHY



```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 2ns
Rx Clock Skew = 2ns
```

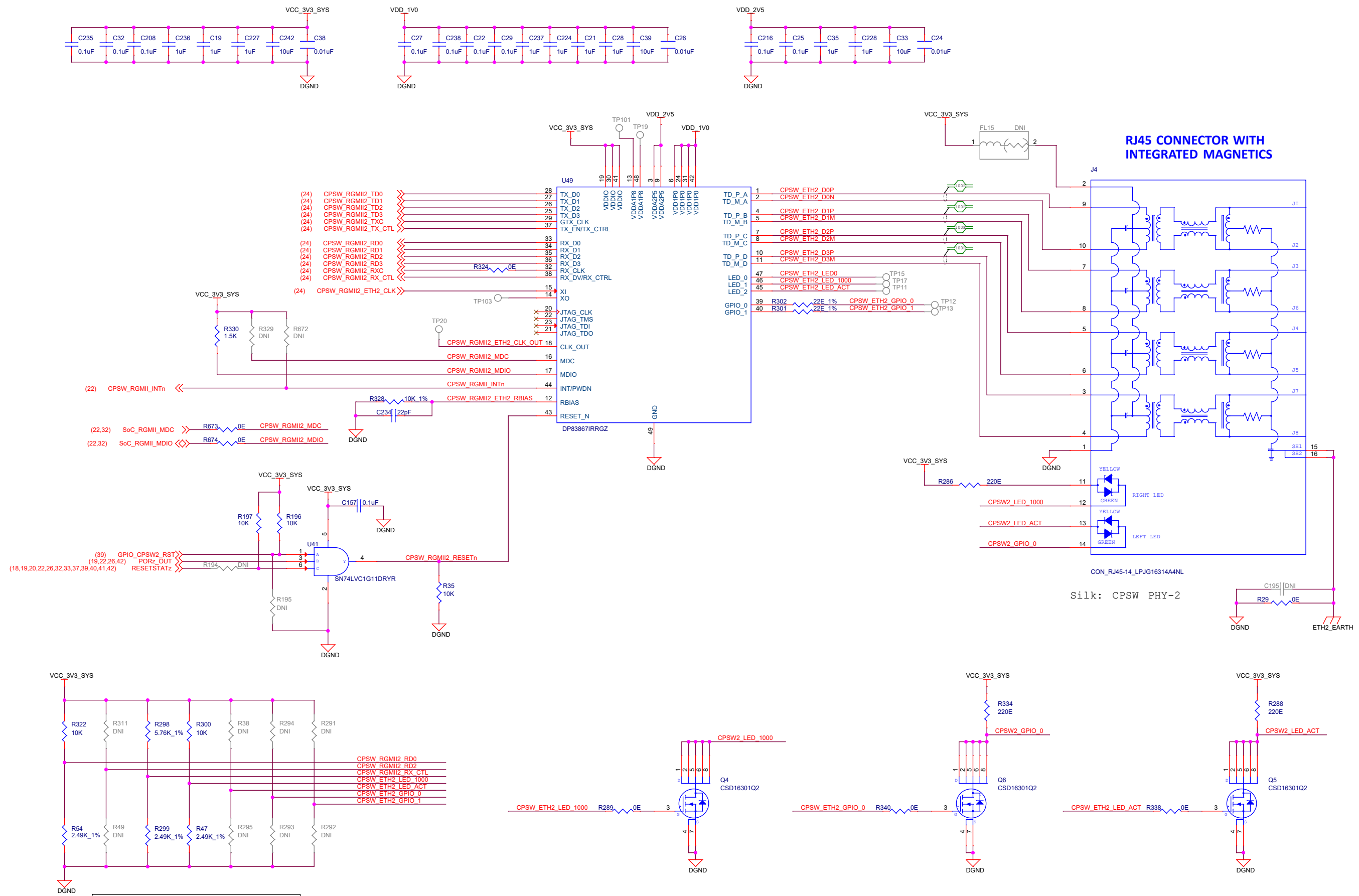
Designed for TI by Mistral Solutions Pvt Ltd



Title	CPSW RGMII_1 ETHERNET PHY
-------	---------------------------

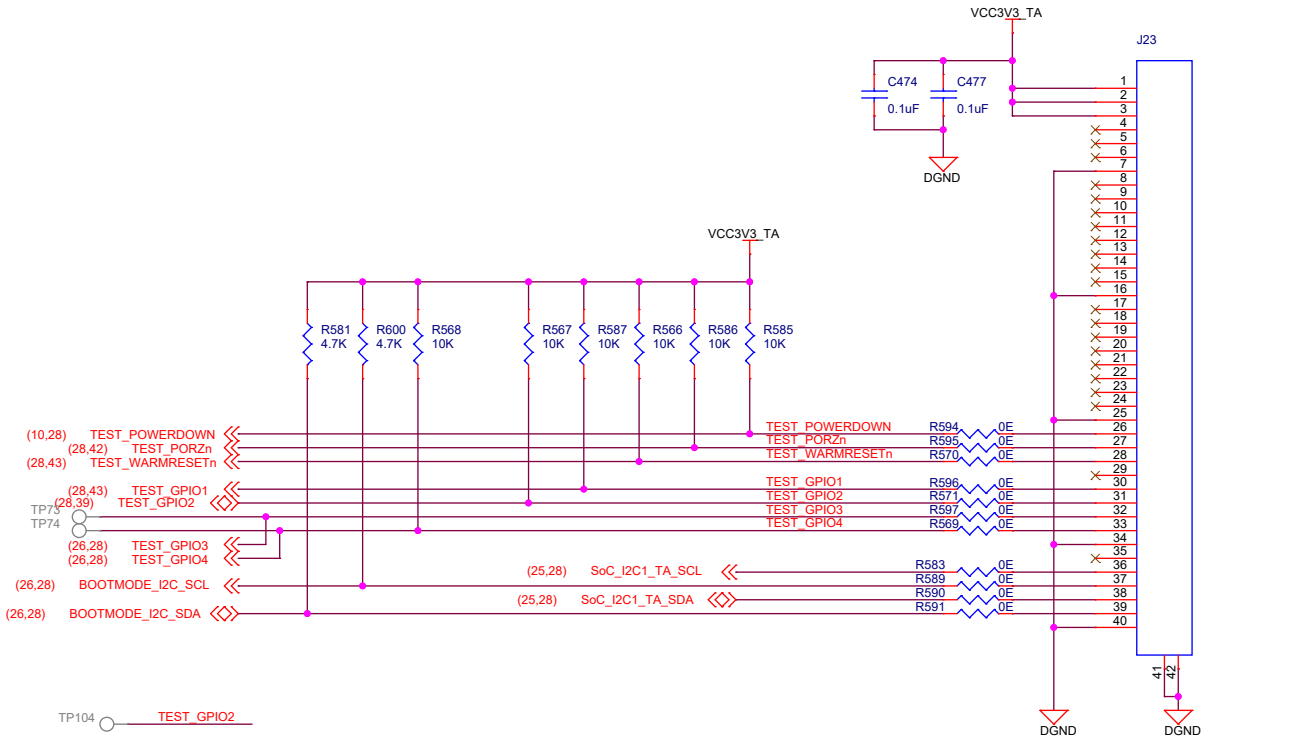
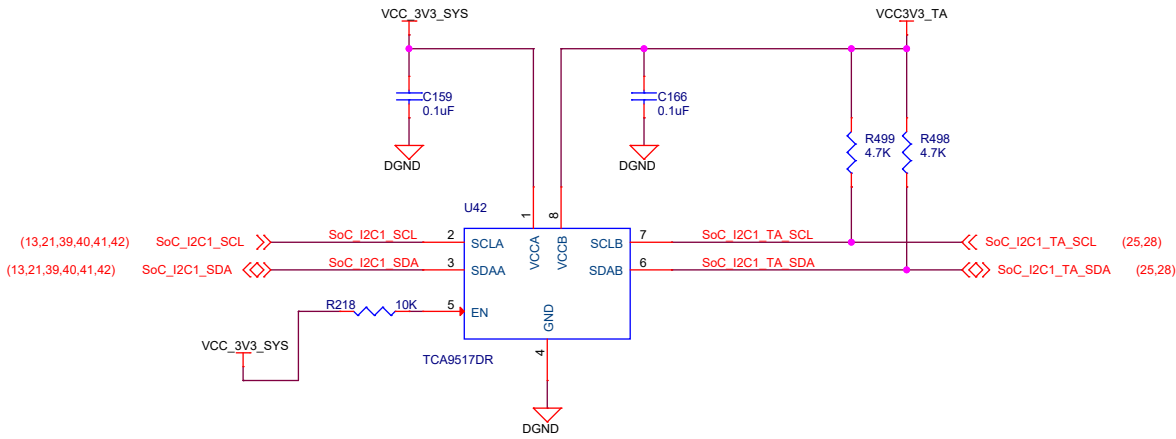
Size	PROC114A(002)	Rev
C		A
Date:	Monday, December 05, 2022	Sheet 22 of 44

CPSW RGMII 2 - PHY



40-PIN TEST AUTOMATION HEADER

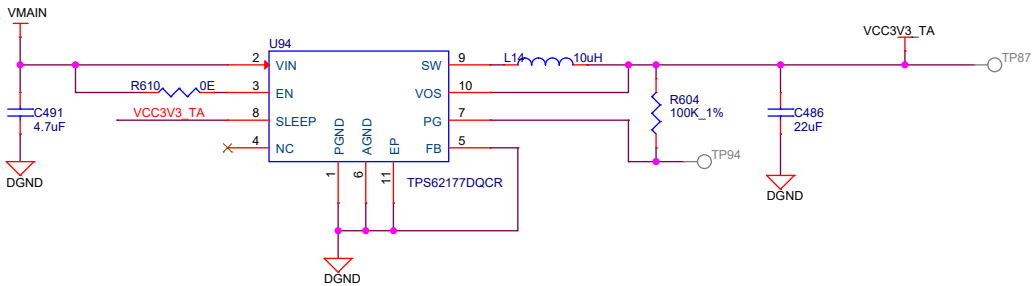
I2C BUS BUFFER



CON_FLEX_40X1_FH12A-40S-0.5SH
Silk: AUTOMATION HDR

TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SoC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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Title TEST AUTOMATION

Size PROC114A(002)

Rev

Date: Monday, December 05, 2022

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BOOTMODE IO EXPANDER

VCC3V3_TA TA

VCC3V3_SYS SYS

C430 0.1uF

DGND

C431 0.1uF

DGND

U75

1

23

24

3

4

5

6

7

8

9

10

2

22

11

12

13

14

15

16

17

18

19

20

21

25

SN74AVC8T245RHL

DIR

BOOTMODEON

DIR1

GND1

GND2

GND3

EP

VCCA

VCCB1

VCCB2

A1

A2

A3

A4

A5

A6

A7

A8

B1

B2

B3

B4

B5

B6

B7

B8

BOOTMODE7

BOOTMODE6

BOOTMODE5

BOOTMODE4

BOOTMODE3

BOOTMODE2

BOOTMODE1

BOOTMODE0

DIR = H: A -> B

DIR = L: B -> A

OE = H: output = Hi-Z

(19,22,23,42) PORz_OUT

R221 DNI

SYSBOOT_BUF_ENz

(18,19,20,22,23,32,33,37,39,40,41,42) RESETSTATz

R222 OE

(25,28) TEST_GPIO3

TEST_GPIO3

[illegible]

Silk: BMODE 0-7

SYS_BOOTMODE0
SYS_BOOTMODE1
SYS_BOOTMODE2
SYS_BOOTMODE3
SYS_BOOTMODE4
SYS_BOOTMODE5
SYS_BOOTMODE6
SYS_BOOTMODE7

R202 100K 1%
R203 100K 1%
R204 100K 1%
R205 100K 1%
R206 100K 1%
R207 100K 1%
R208 100K 1%
R209 100K 1%

1 2 3 4 5 6 7 8

9 10 11 12 13 14 15 16

R236 1K 1%
R237 1K 1%
R238 1K 1%
R239 1K 1%
R240 1K 1%
R241 1K 1%
R242 1K 1%
R243 1K 1%

VCC3V3_TA

SW1 416131160808

DGND

The diagram shows the SW2 switch (416131160808) with pins 1 through 8. The connections are as follows:

- Pin 1:** Connected to CPU pin R210 (100K 1%) to DGN1.
- Pin 2:** Connected to CPU pin R211 (100K 1%) to DGN1.
- Pin 3:** Connected to CPU pin R212 (100K 1%) to DGN1.
- Pin 4:** Connected to CPU pin R213 (100K 1%) to DGN1.
- Pin 5:** Connected to CPU pin R214 (100K 1%) to DGN1.
- Pin 6:** Connected to CPU pin R215 (100K 1%) to DGN1.
- Pin 7:** Connected to CPU pin R216 (100K 1%) to DGN1.
- Pin 8:** Connected to CPU pin R217 (100K 1%) to DGN1.
- Pin 9:** Connected to CPU pin R220 (1K 1%) to SW2 pin 9.
- Pin 10:** Connected to CPU pin R221 (1K 1%) to SW2 pin 10.
- Pin 11:** Connected to CPU pin R248 (1K 1%) to SW2 pin 11.
- Pin 12:** Connected to CPU pin R249 (1K 1%) to SW2 pin 12.
- Pin 13:** Connected to CPU pin R247 (1K 1%) to SW2 pin 13.
- Pin 14:** Connected to CPU pin R246 (1K 1%) to SW2 pin 14.
- Pin 15:** Connected to CPU pin R244 (1K 1%) to SW2 pin 15.
- Pin 16:** Connected to CPU pin R245 (1K 1%) to SW2 pin 16.

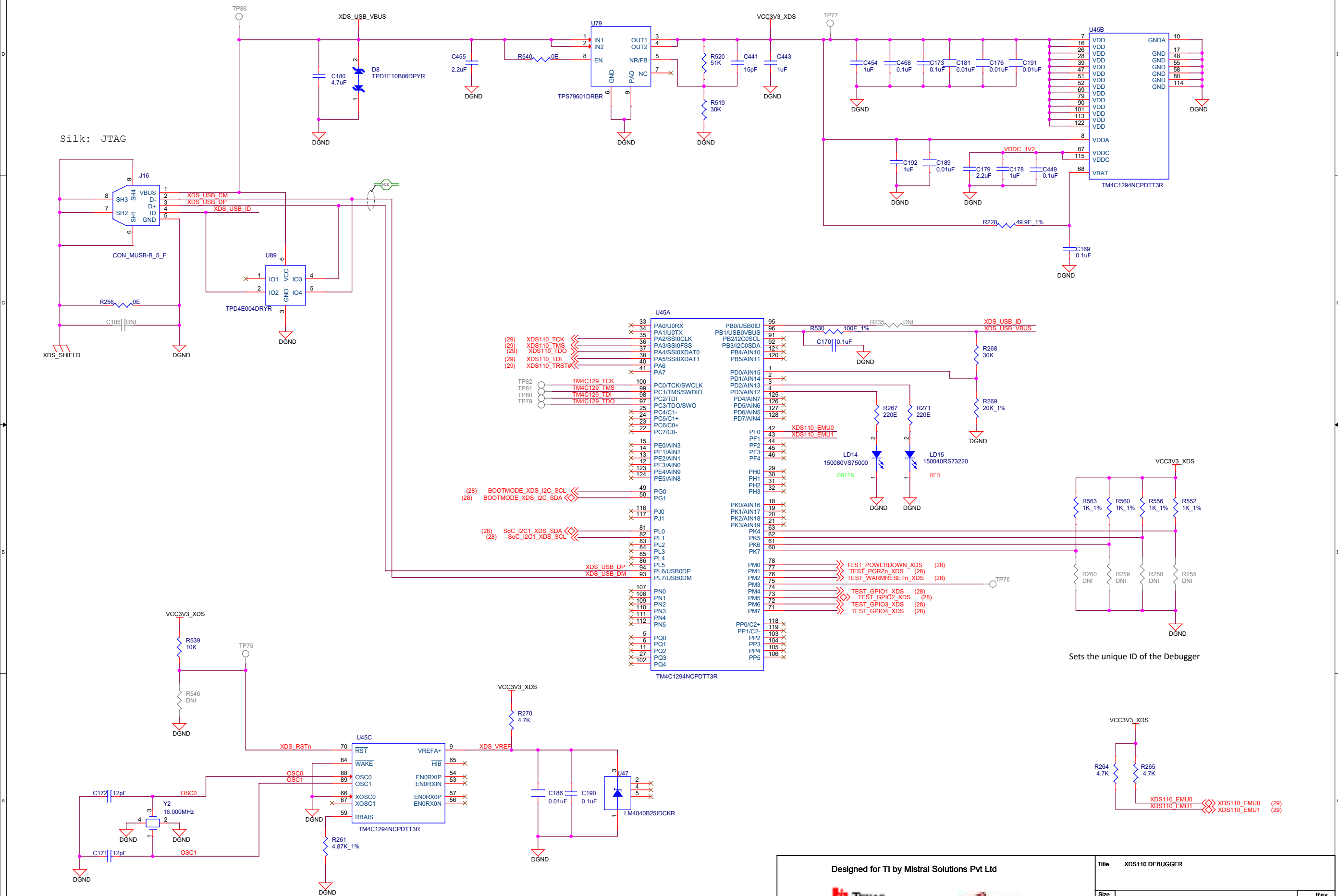
Additional labels in the diagram include:

- SW2:** 416131160808
- VCC3V3:** TA
- DGN1:** DGN1
- Legend:**
 - H ON = LOGIC 1
 - H OFF = LOGIC 0
- Silk:** BMODE 8-15

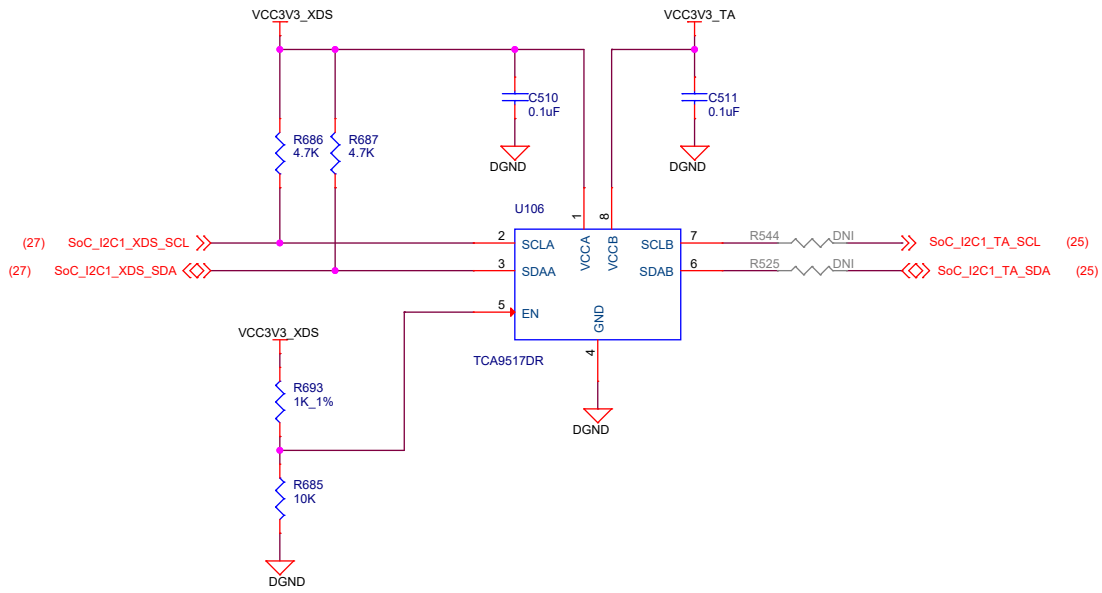


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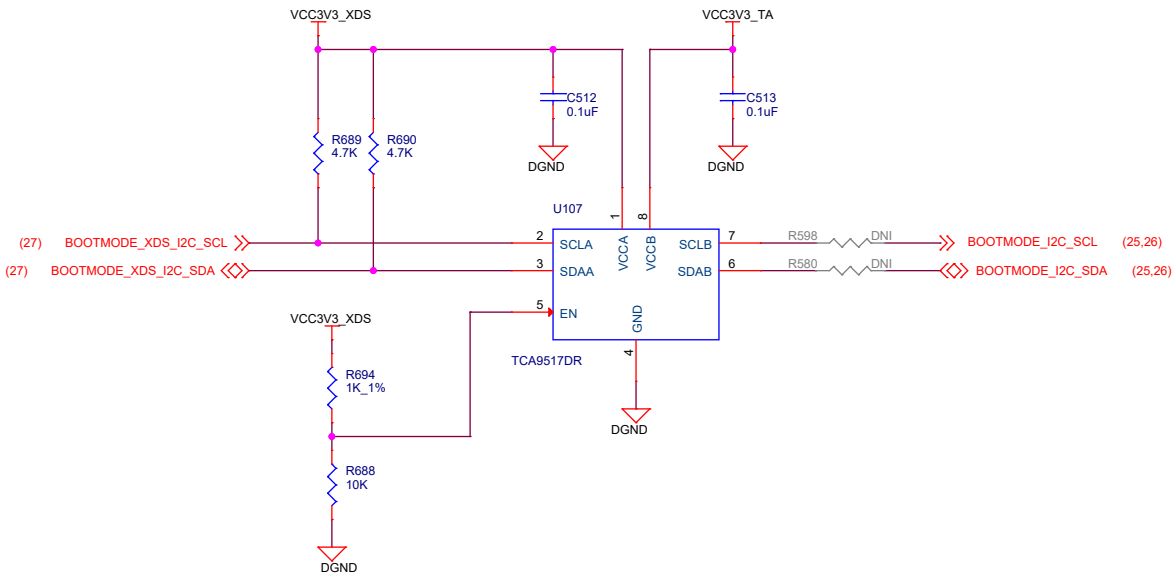
XDS110 DEBUGGER



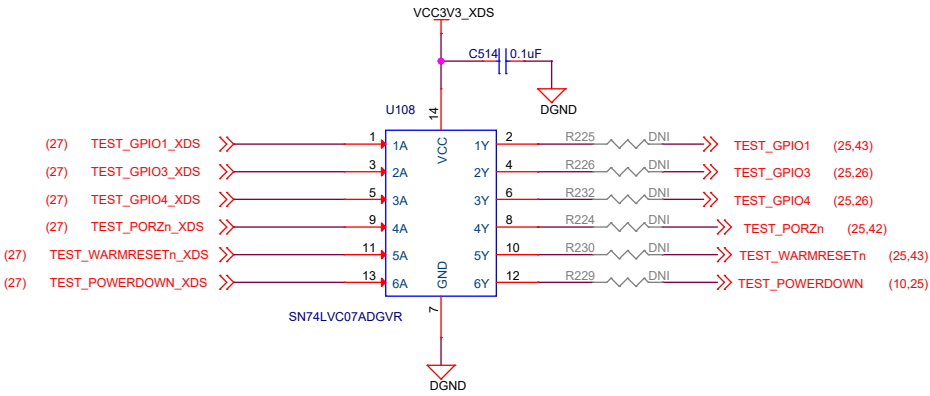
I2C_TA BUS BUFFER



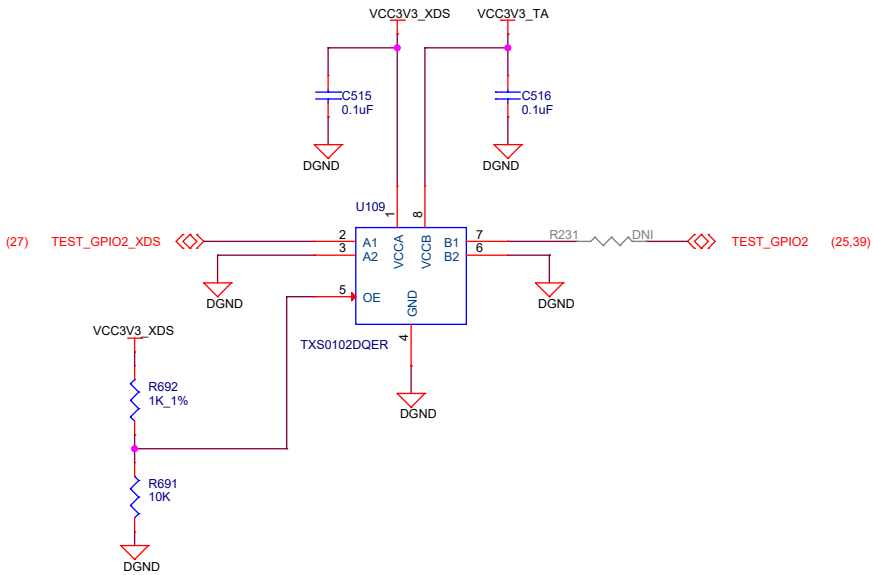
BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS



Pull ups(R567, R587, R517, R568, R585, R586 & R566) to VCC3V3_TA are present

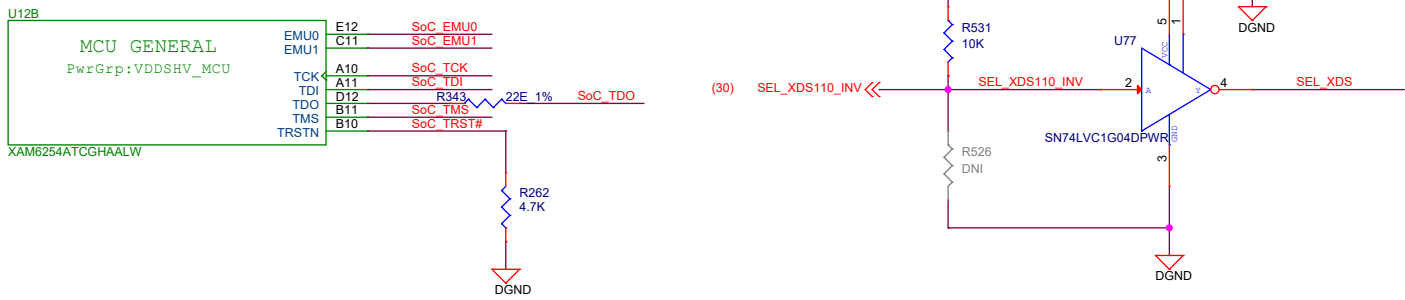


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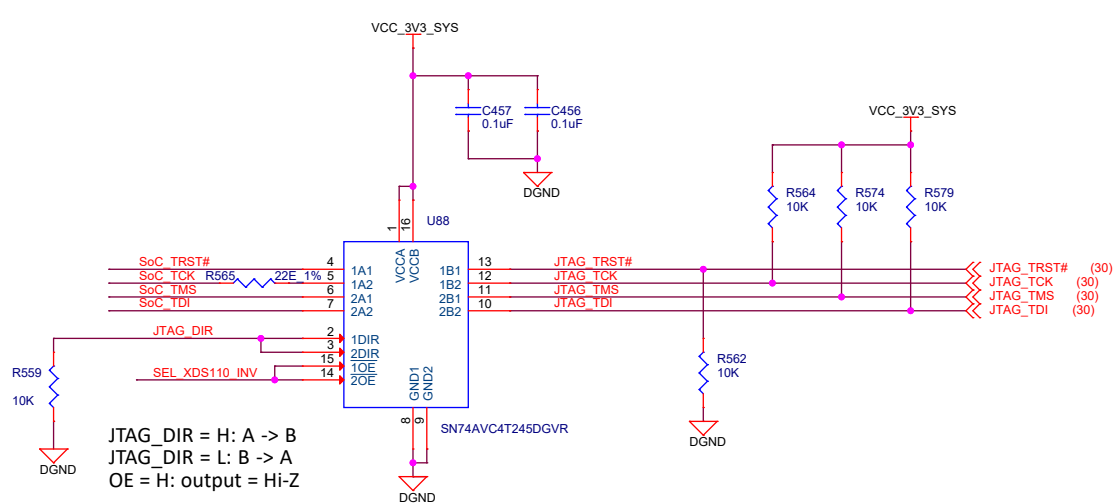


Title AUTOMATION SIGNALS BUFFER		
Size	PROC114A(002)	Rev
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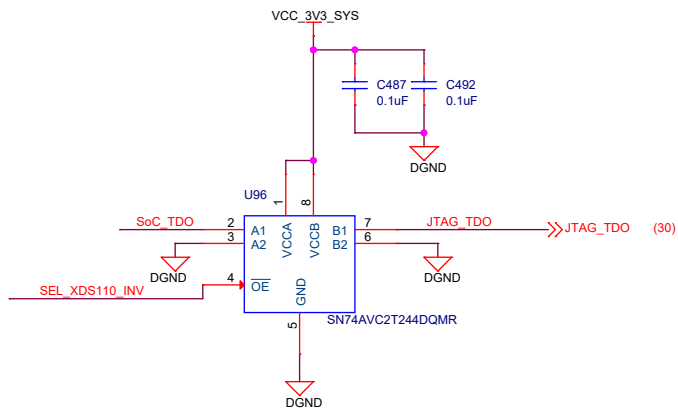
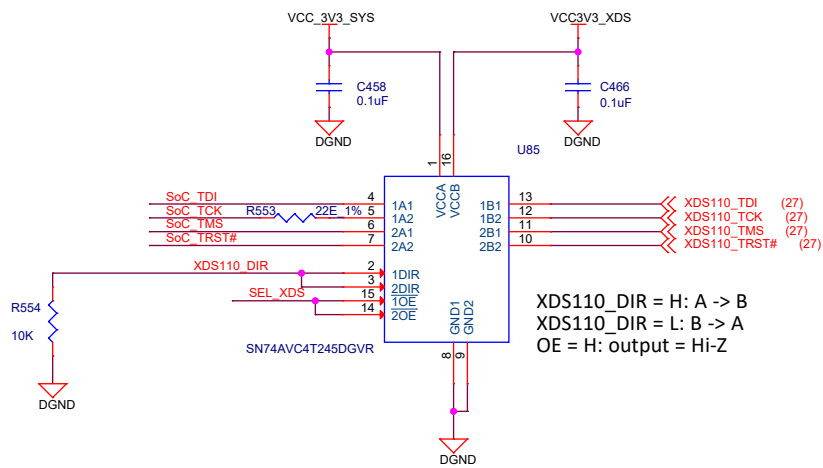
JTAG SOC SECTION



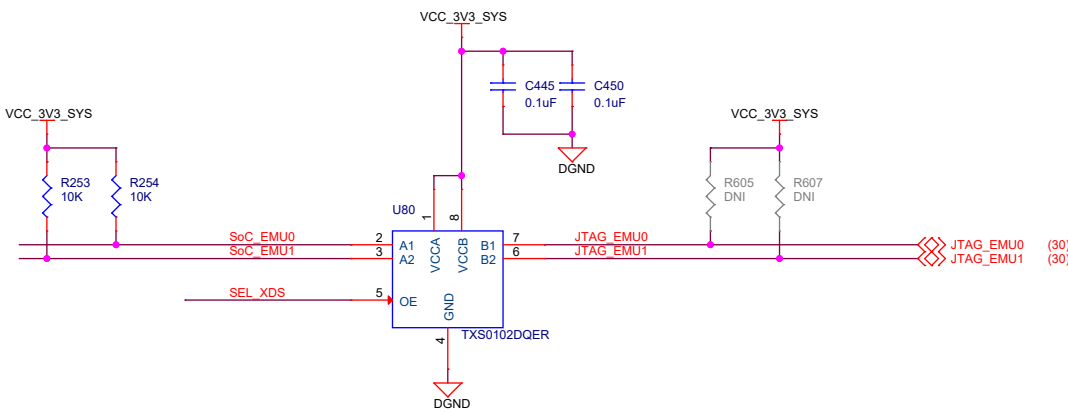
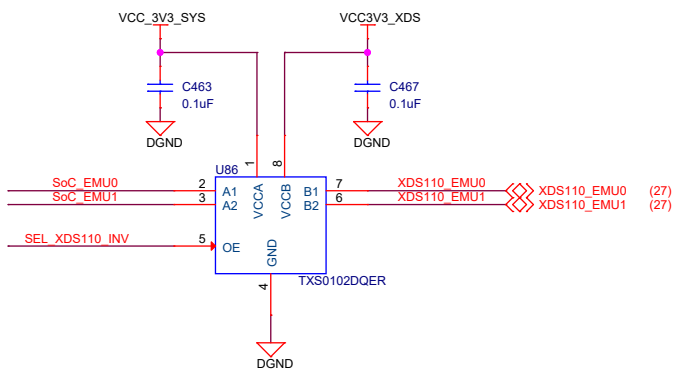
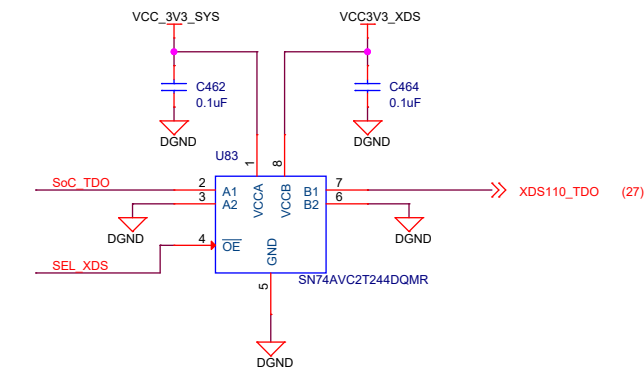
cTI20 JTAG BUFFERS



BUFFER XDS110



CAD NOTE: Buffers U88 and U96 need to be placed closer to the cTI-20pin connector J17 to reduce Stub length of the JTAG signals.

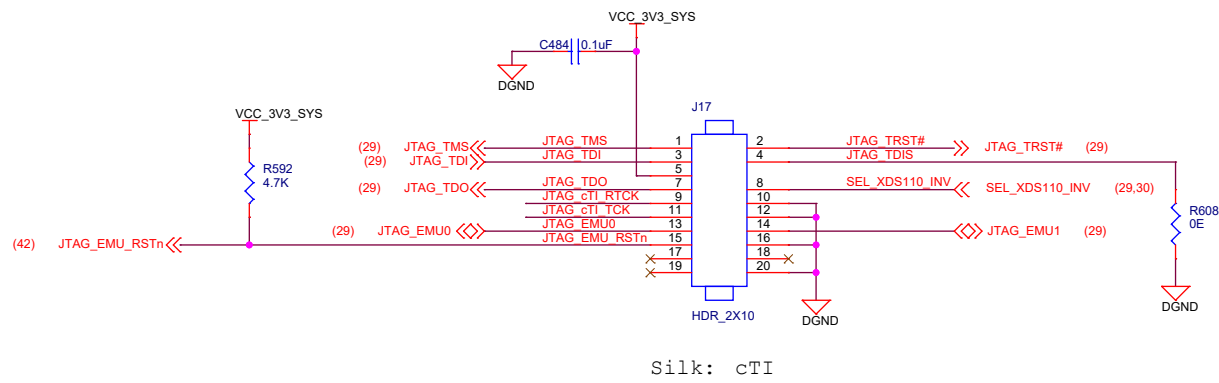


Designed for T1 by Mistral Solutions Pvt Ltd

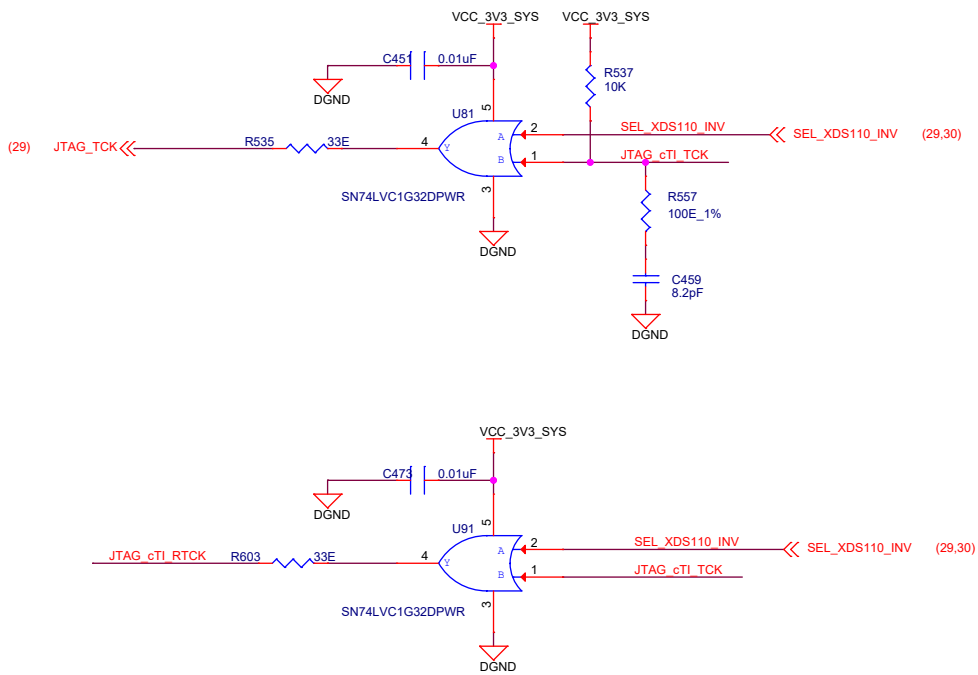


Title		JTAG BUFFER	
Size	PROC114A(002)	Rev	
C		A	
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JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER



Designed for TI by Mistral Solutions Pvt Ltd



Title JTAG 20 PIN cTI CONNECTOR

Size PROC114A(002)

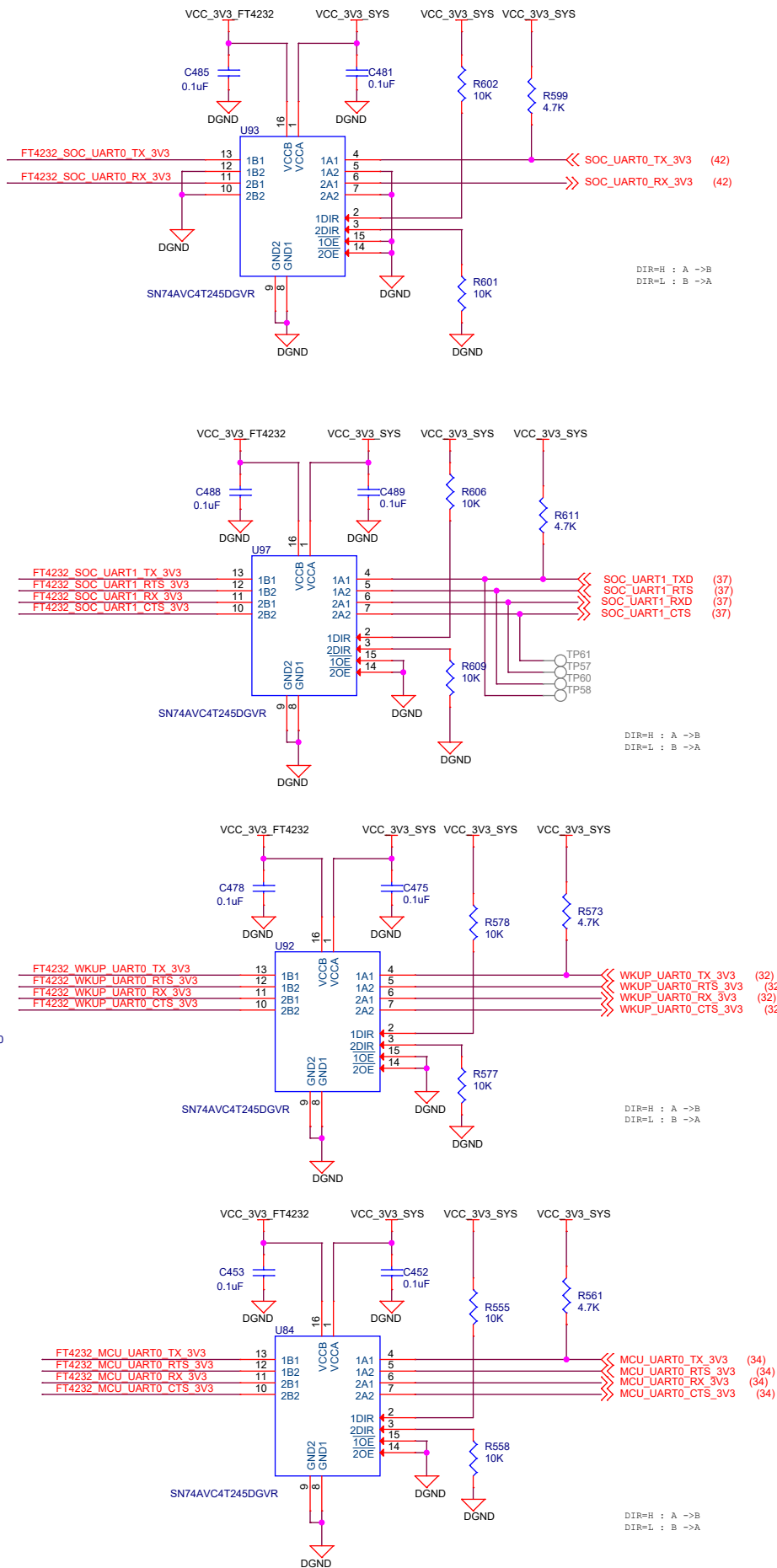
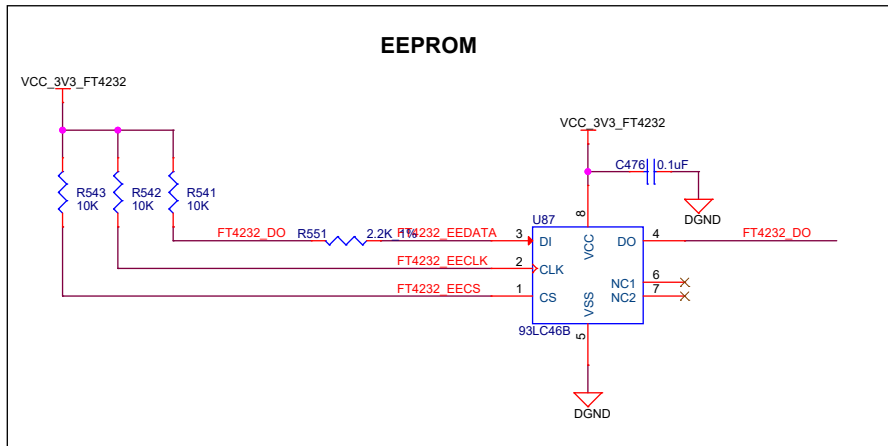
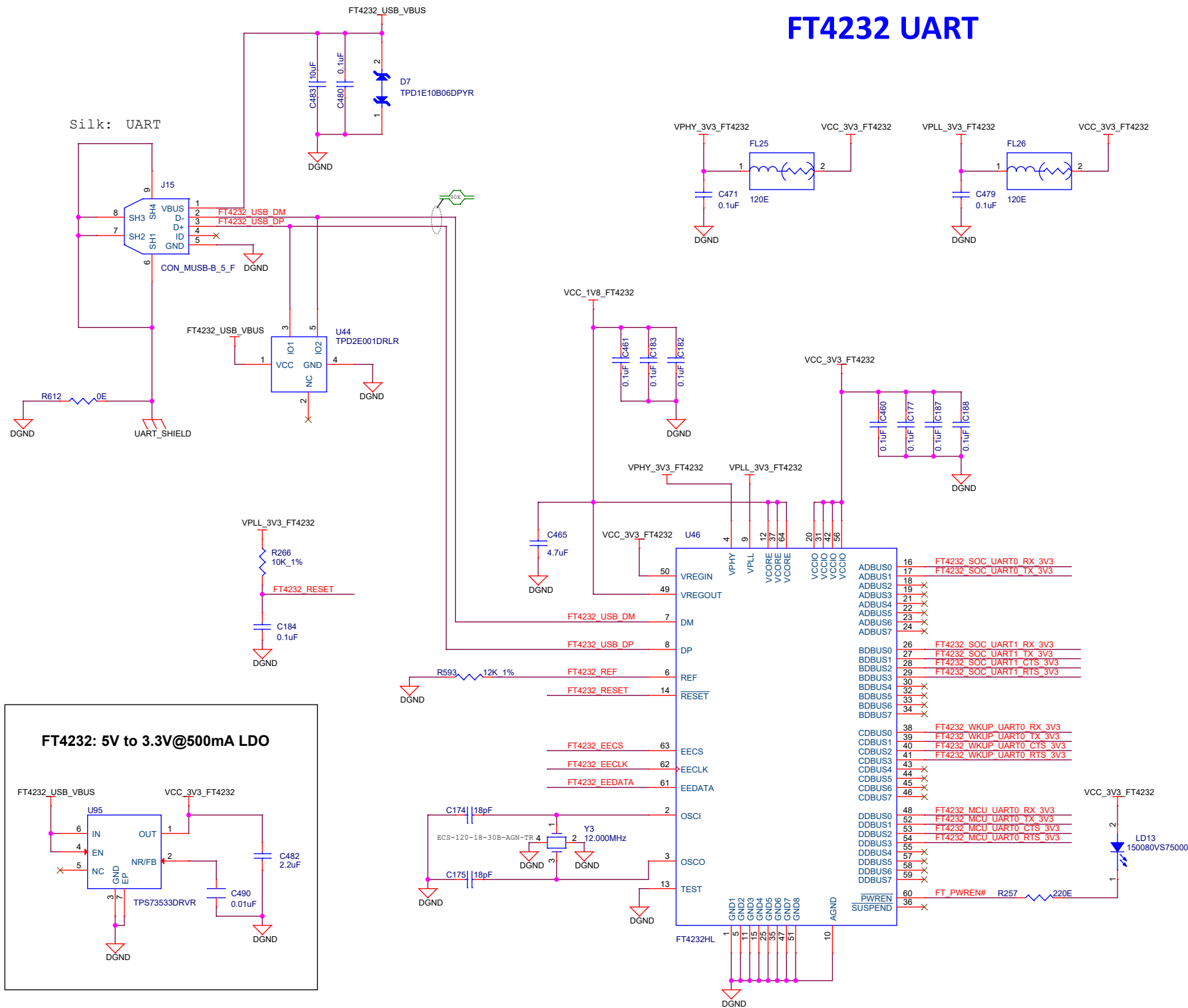
Rev

A

Date: Monday, December 05, 2022

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FT4232 UART

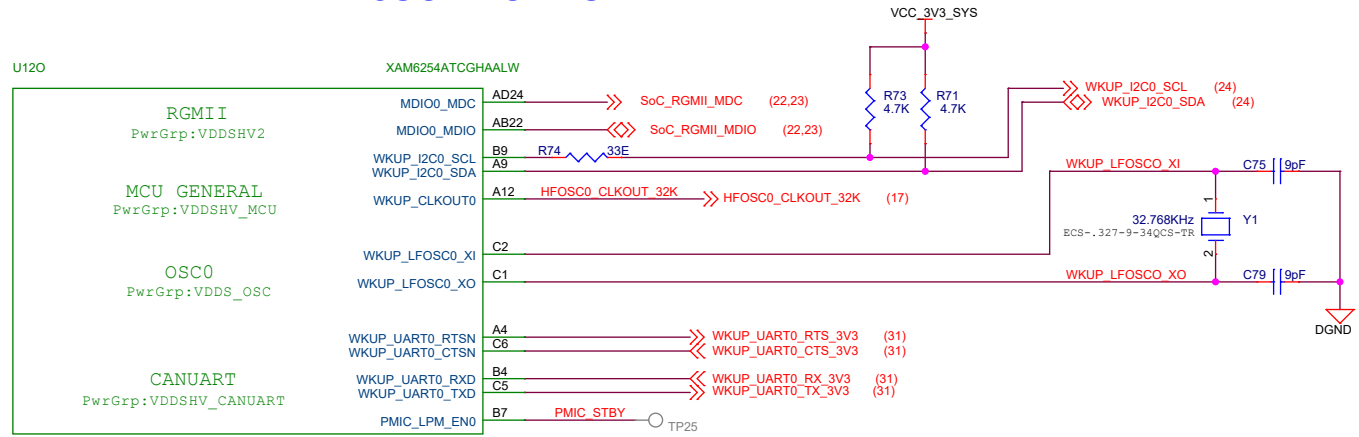


Designed for TI by Mistral Solutions Pvt Ltd

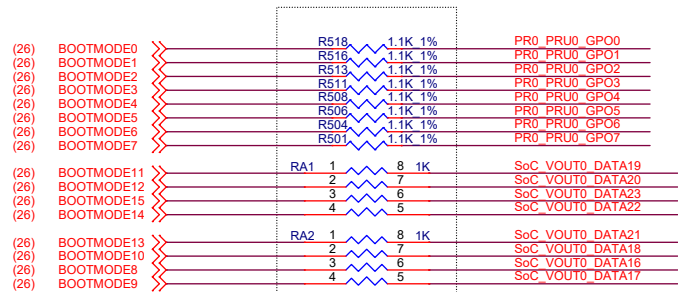


Title				FT4232 UART TO USB BRIDGE			
Size		PROC114A(002)				Rev	
C						A	
Date:		Monday, December 05, 2022		Sheet		31 of 44	

SOC WKUP DOMAIN

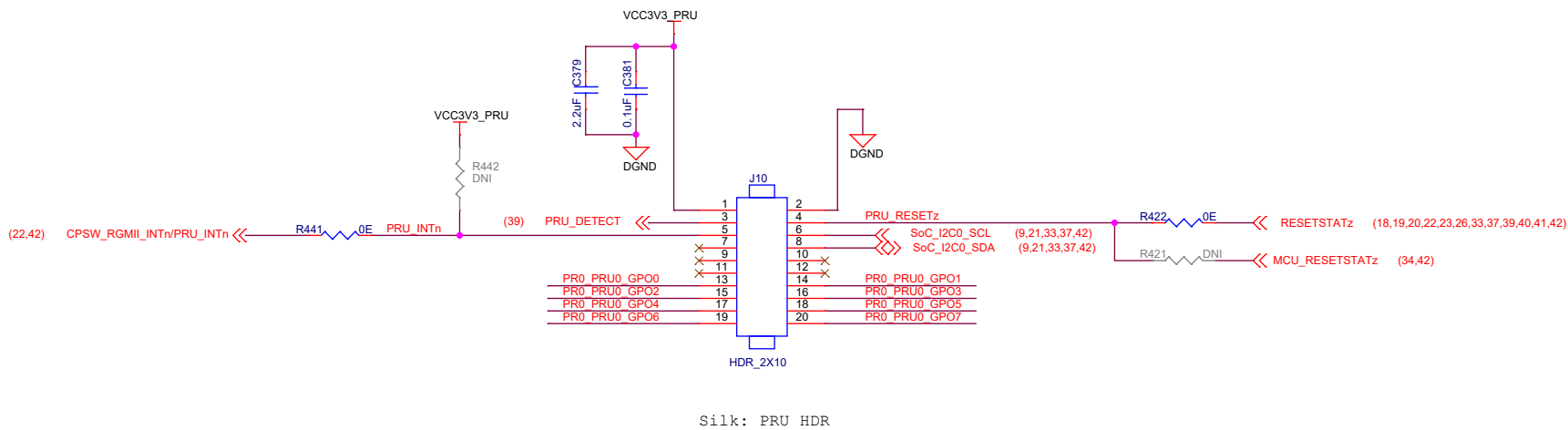


BOOTMODE PINS



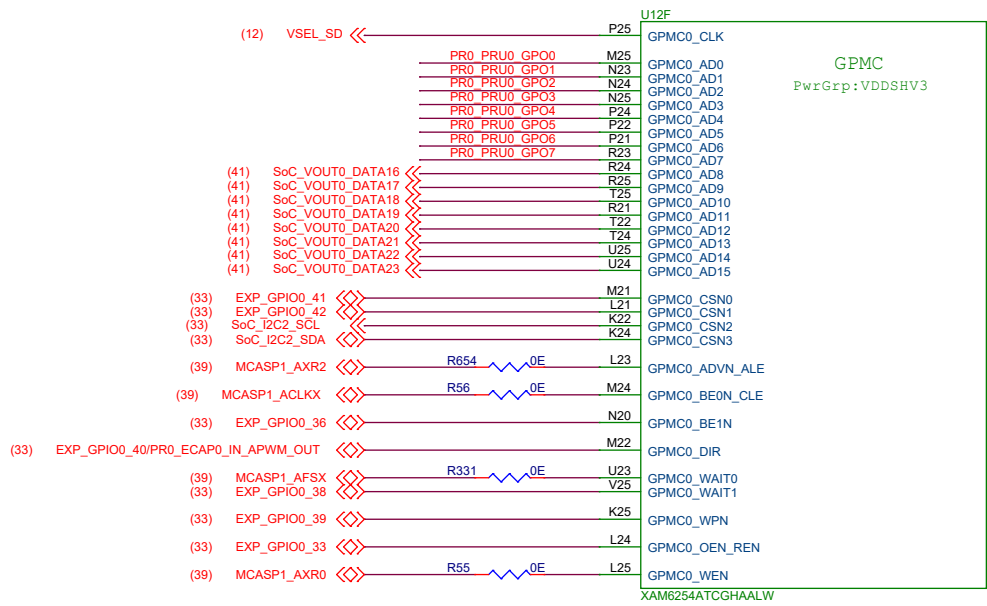
NOTE: Resistors are used to isolate the BOOTMODE control logic after the value is latched

PRU HEADER

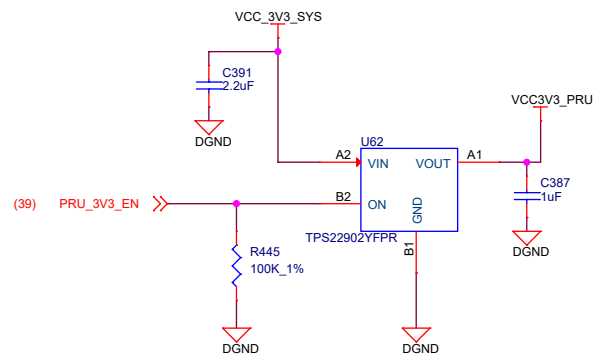


NOTE: PRU Header I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

SOC GPMC



POWER SWITCH FOR PRU HEADER



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Title PRU HEADER

Size PROC114A(002)

C

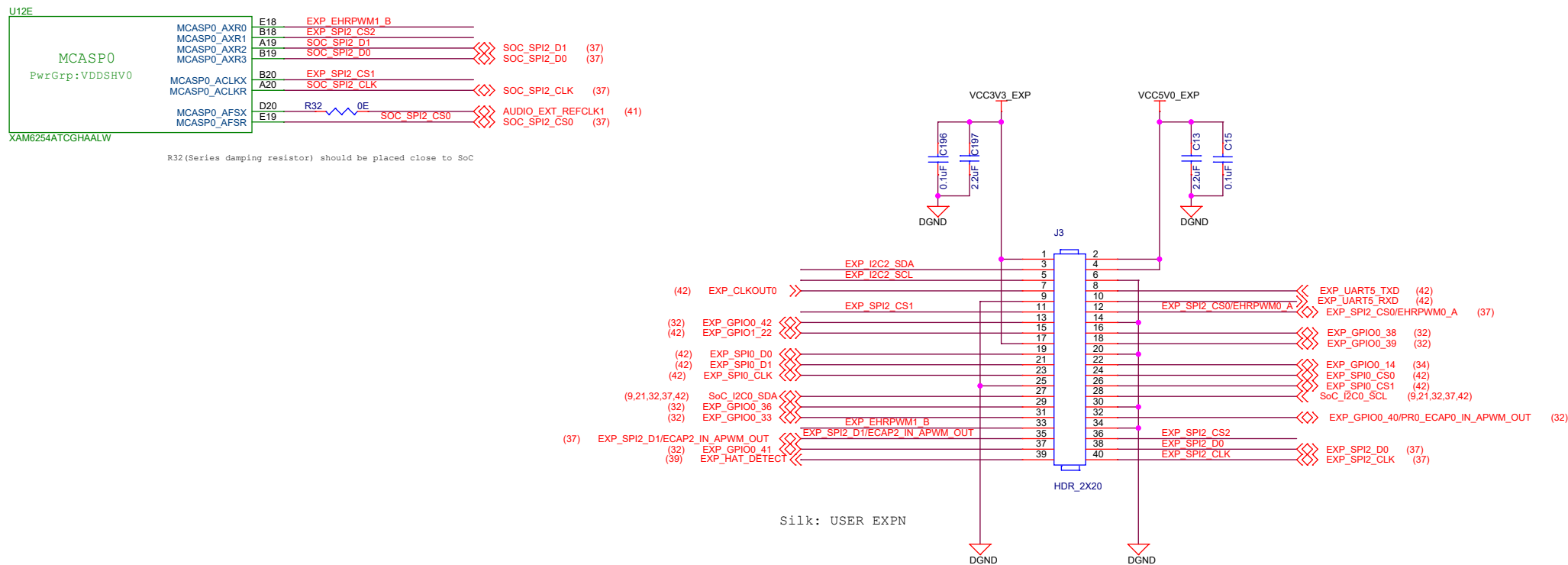
Date: Monday, December 05, 2022

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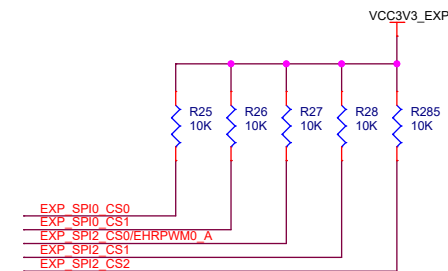
Rev

A

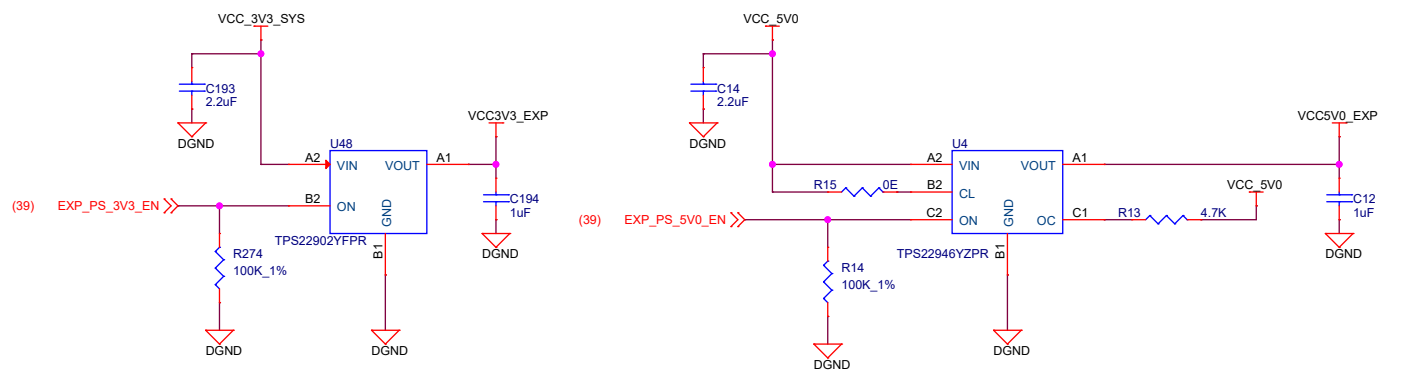
USER EXPANSION CONNECTOR



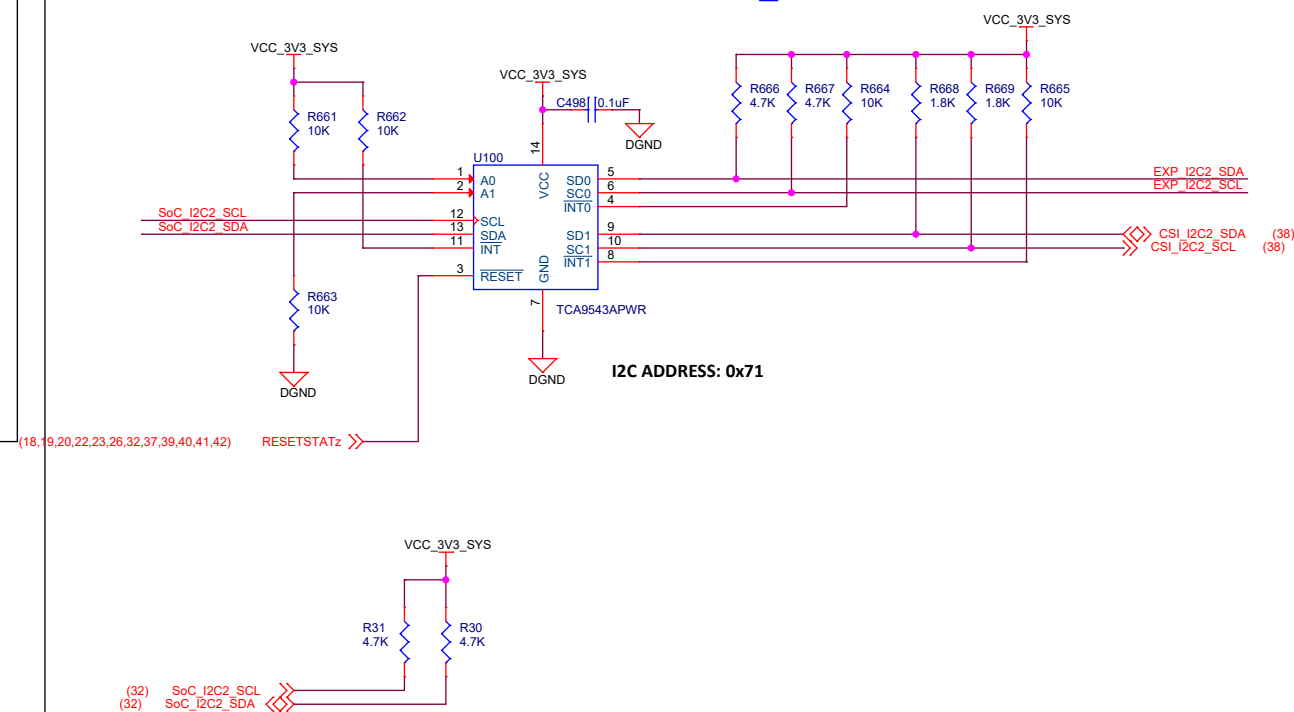
Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



POWER SWITCHES FOR USER EXPANSION CONNECTOR



I2C SWITCH FOR SoC_I2C2



NOTE:

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

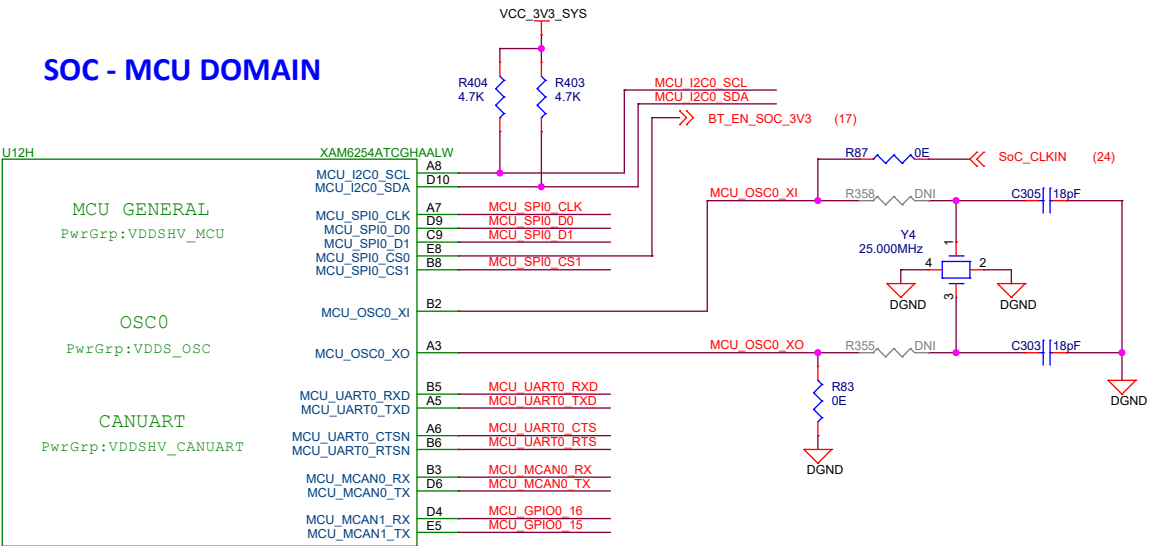
3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

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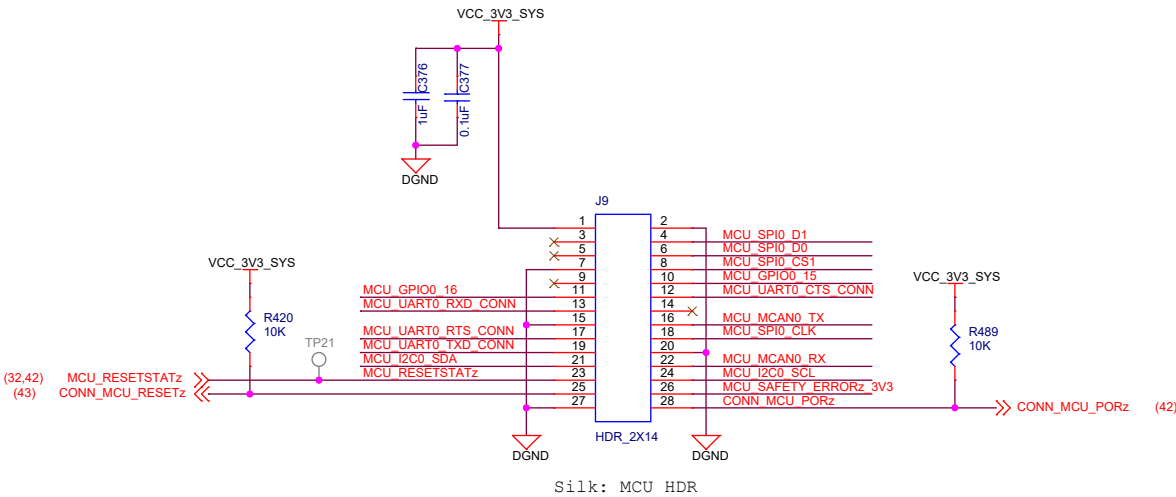


Title				USER EXPANSION CONNECTOR			
Size		PROC114A(002)				Rev	
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Date:		Wednesday, December 07, 2022		Sheet		33 of 44	

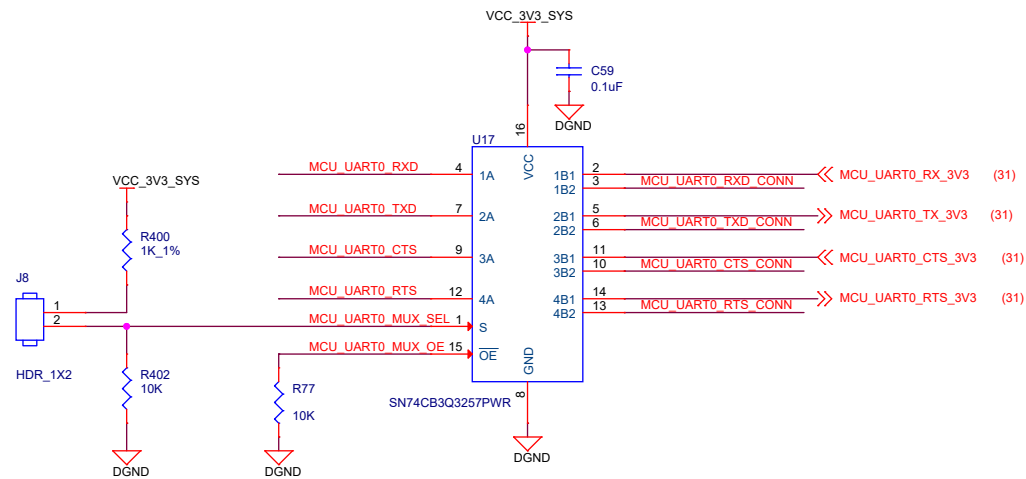
SOC - MCU DOMAIN



MCU HEADER



MCU_UART0 MUX



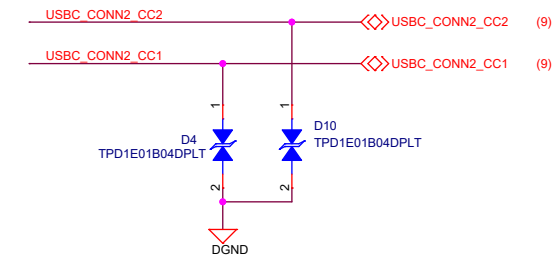
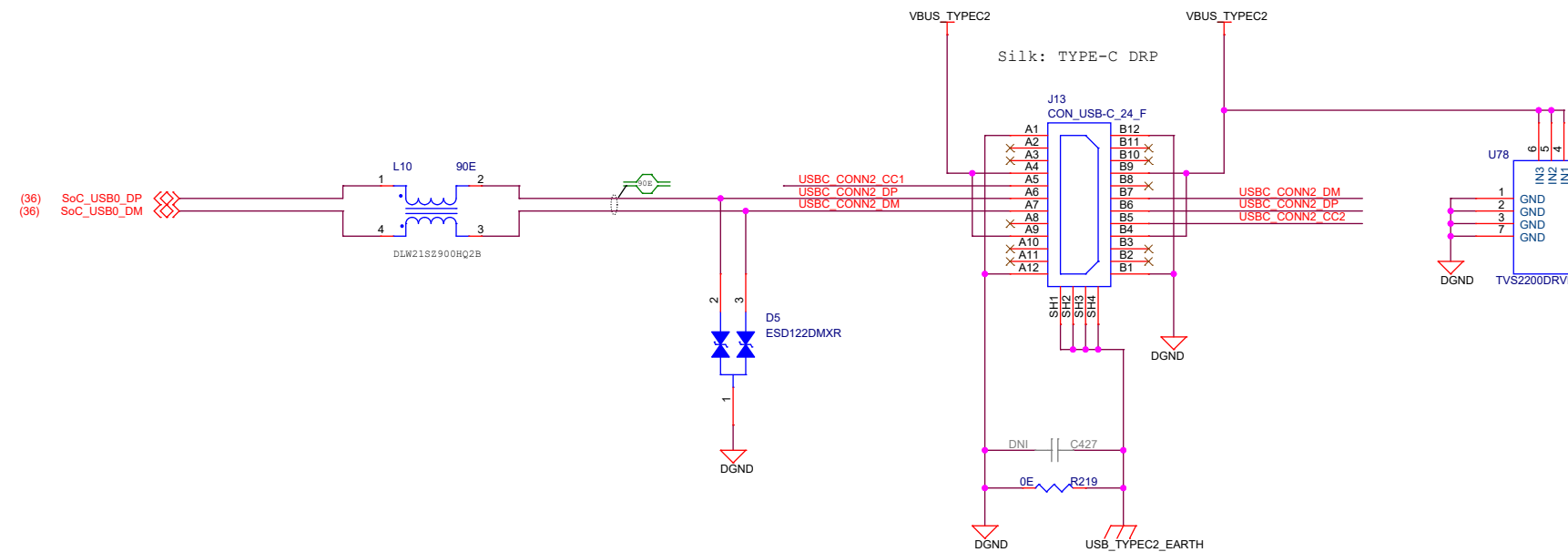
OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

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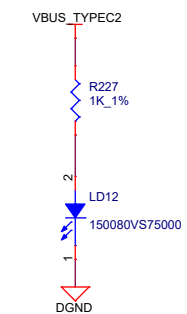


Title		MCU HEADER	
Size	PROC114A(002)	Rev	
C		A	
Date:	Monday, December 05, 2022	Sheet	34 of 44

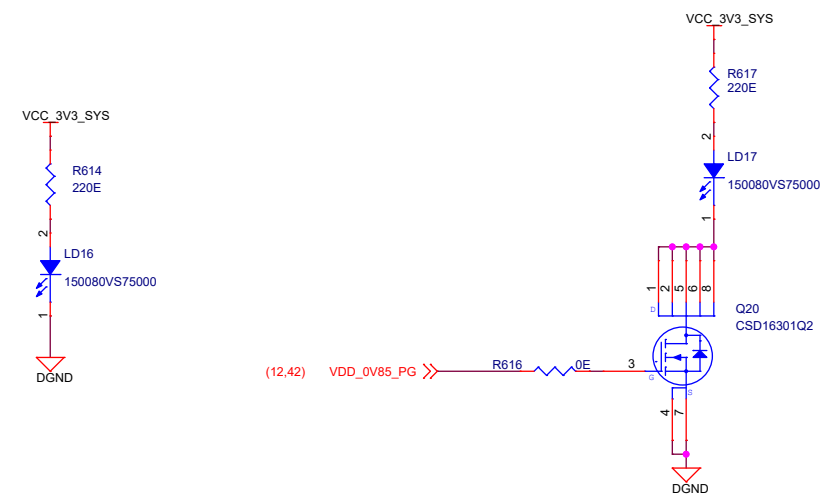
USB0 TYPE-C DRP



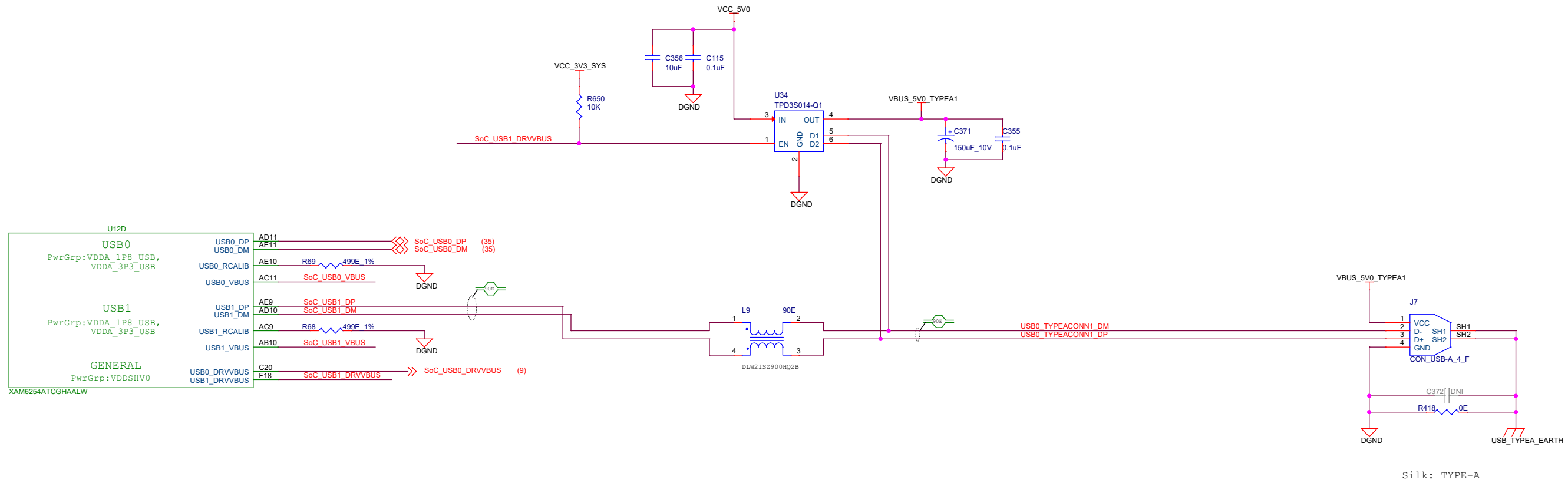
POWER INDICATION LED: VBUS_TYPEC2



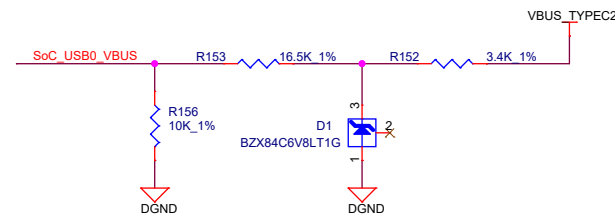
POWER RAIL LEDS



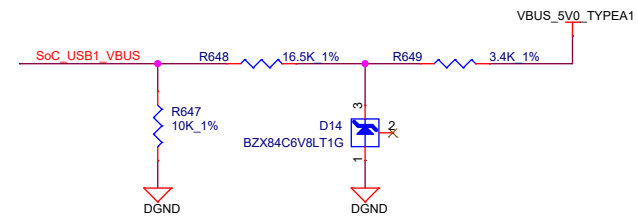
USB1 TYPE-A



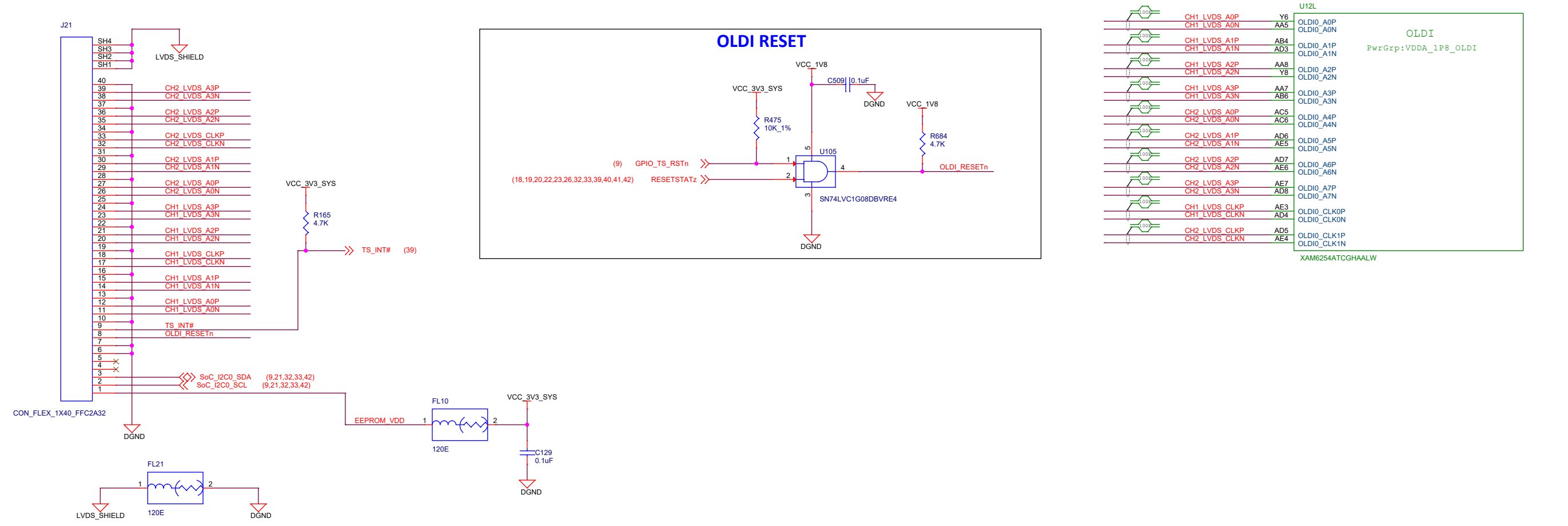
Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



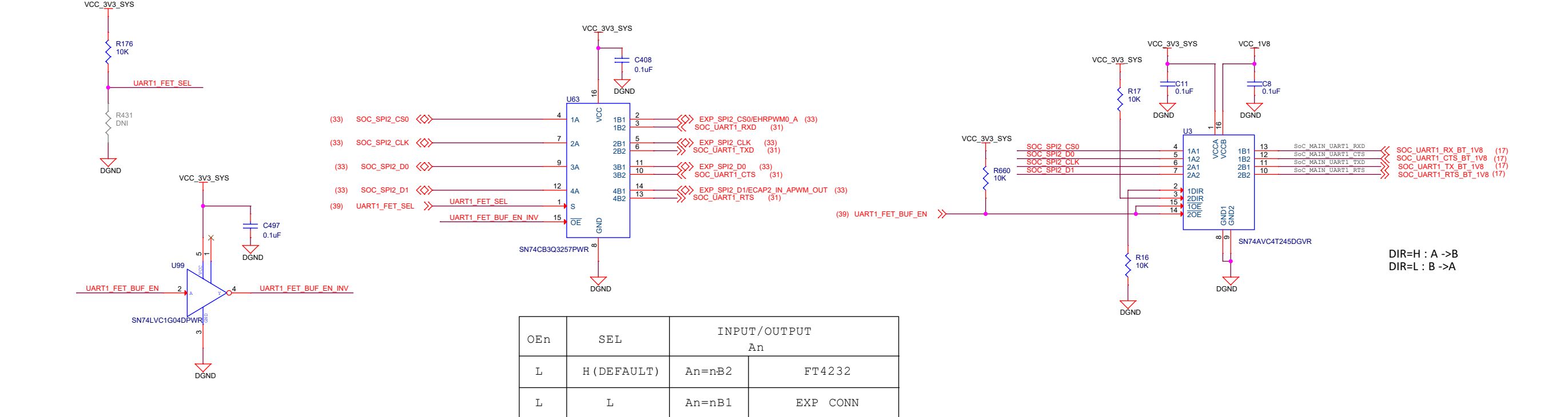
Note: Recommended VBUS circuit for SoC_USB1_VBUS



OLDI DISPLAY INTERFACE



SoC UART1 FET SWITCH & BUFFER



Designed for T1 by Mistral Solutions Pvt Ltd



Title OLDI DISPLAY INTERFACE

Size PROC114A(002)

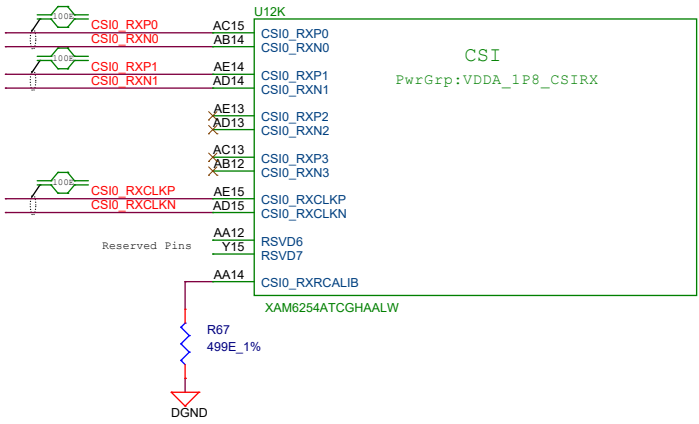
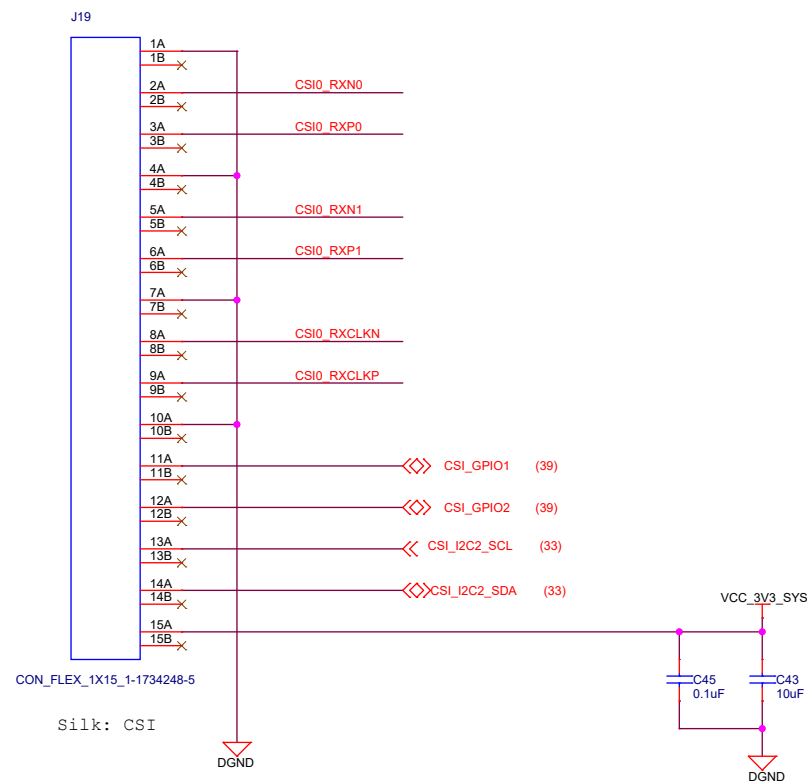
Rev

Date: Monday, December 05, 2022

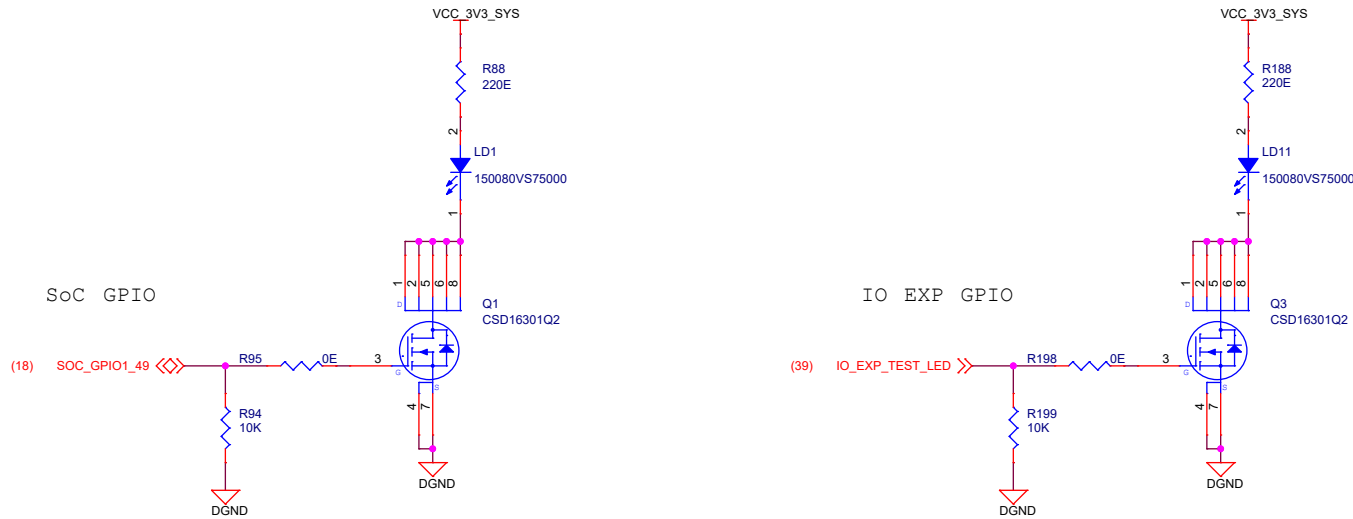
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CSI INTERFACE

CSI CAMERA HEADER



USER TEST LEDS

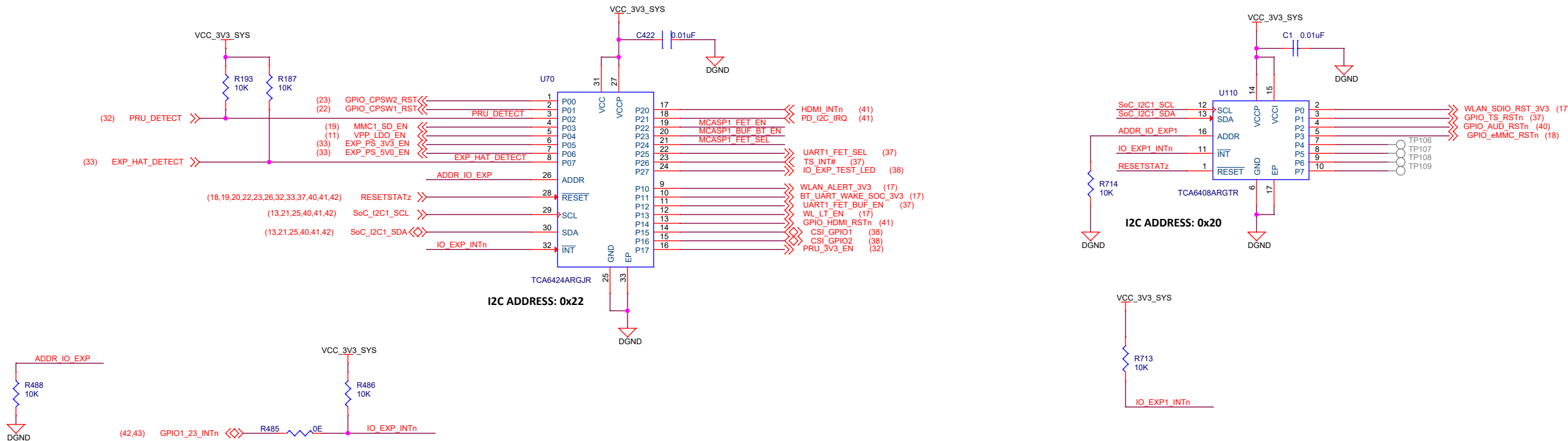


Designed for T1 by Mistral Solutions Pvt Ltd

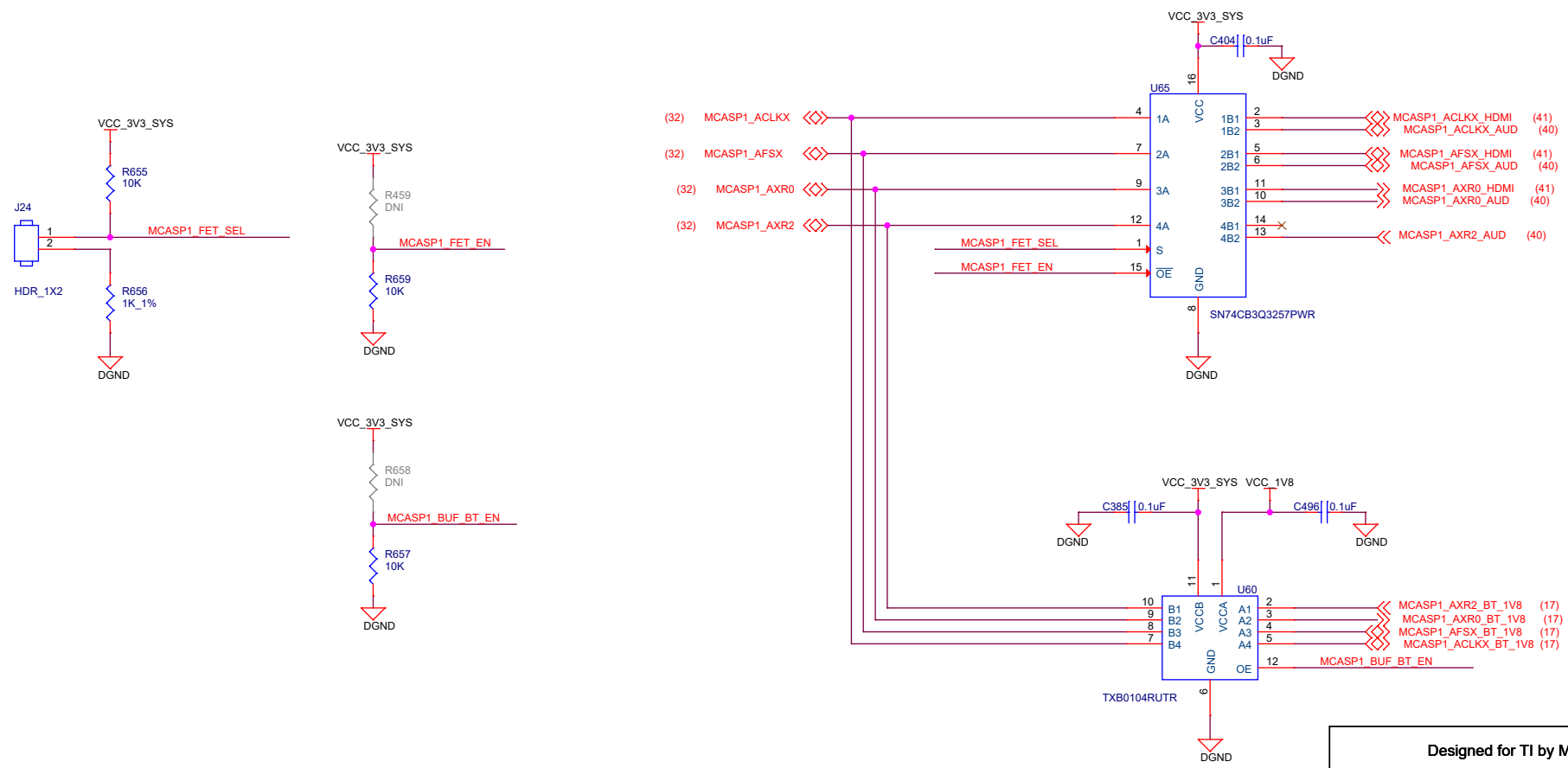


Title CSI INTERFACE & USER TEST LEDS		
Size	PROC114A(002)	Rev
C		A
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IO EXPANDER



MCASP1 FET SWITCH & BUFFER



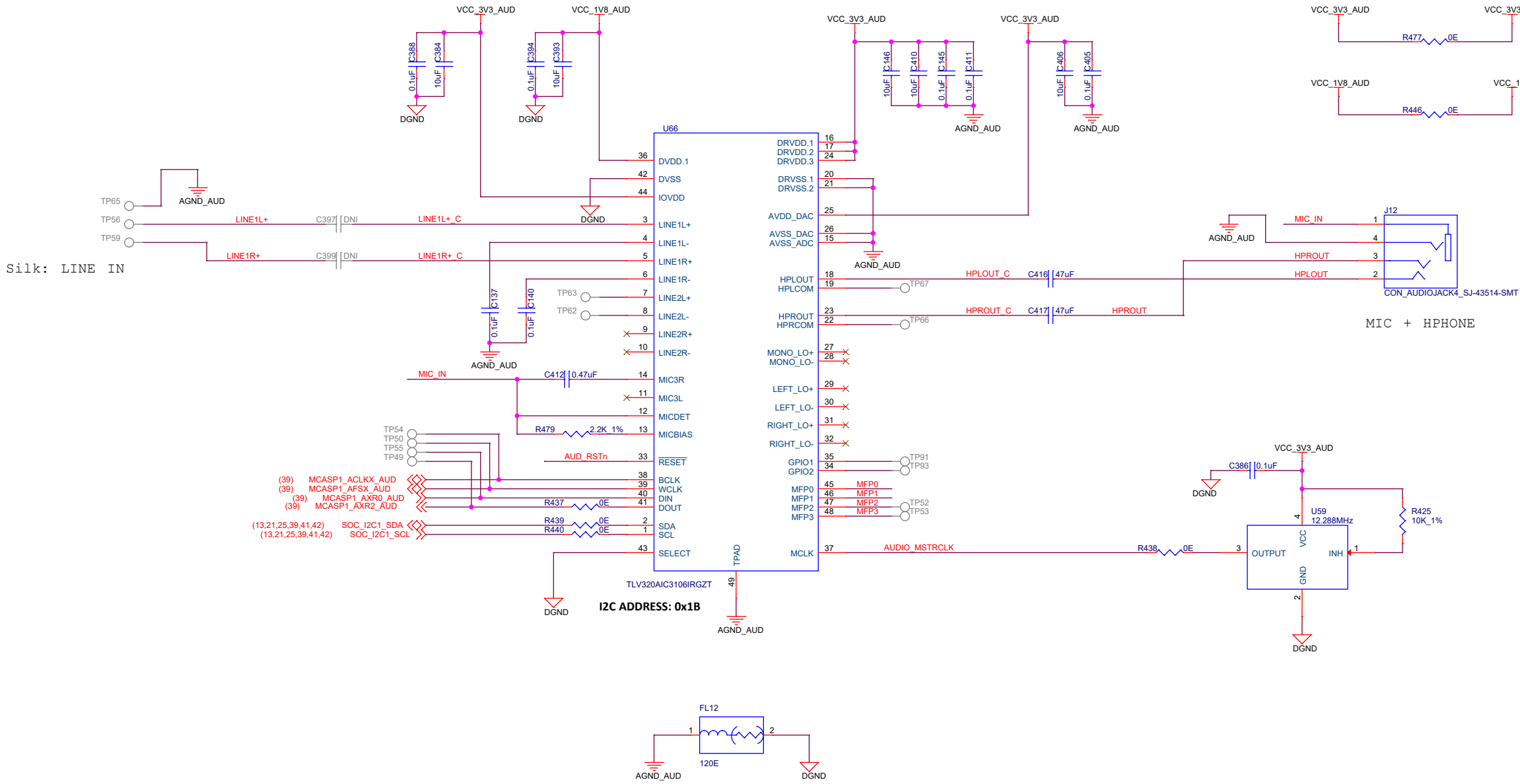
OEn	SEL	INPUT/OUTPUT An	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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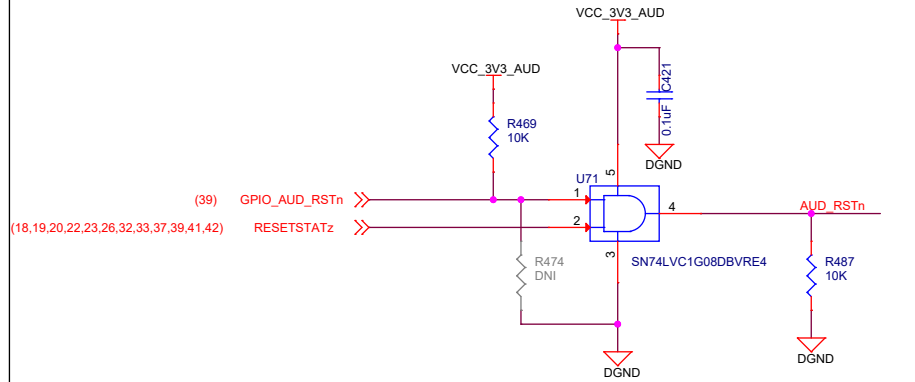


Title IO EXPANDER		
Size C	PROC114A(002)	Rev A
Date: Monday, December 05, 2022	Sheet 39 of 44	

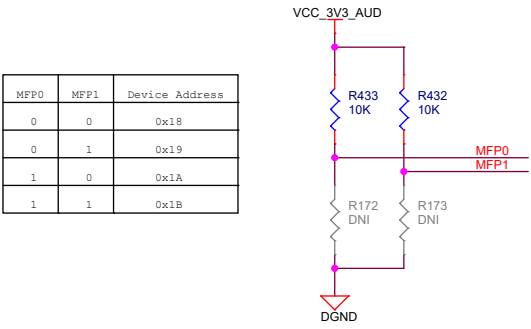
AUDIO CODEC



AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION



MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B

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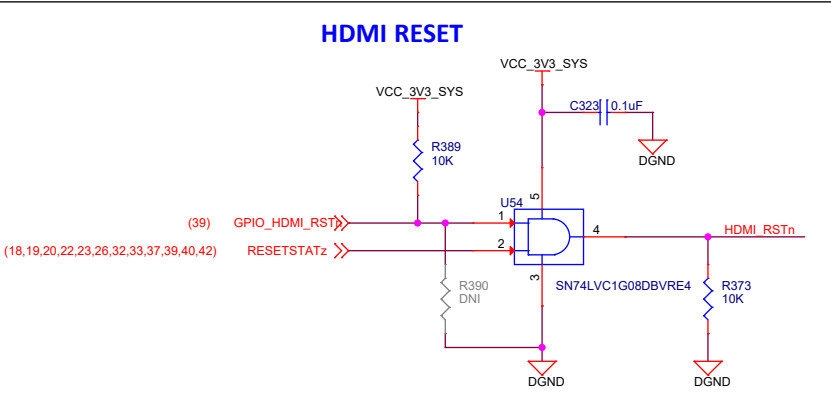
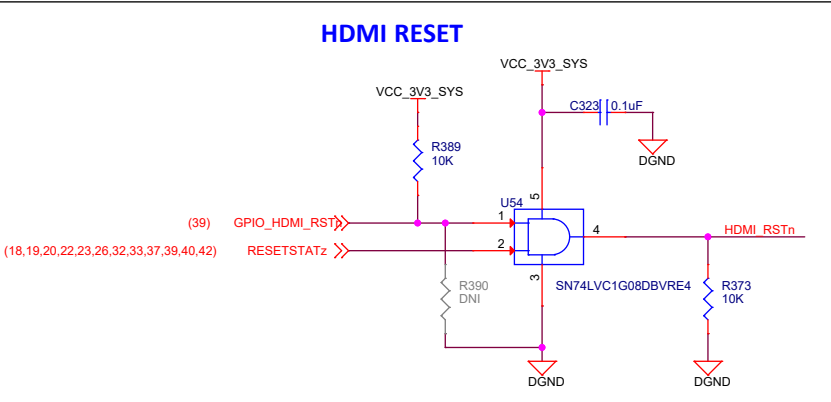
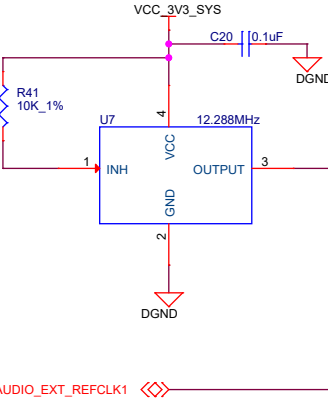
Title AUDIO CODEC		
Size	PROC114A(002)	Rev
C		A
Date:	Monday, December 05, 2022	Sheet 40 of 44

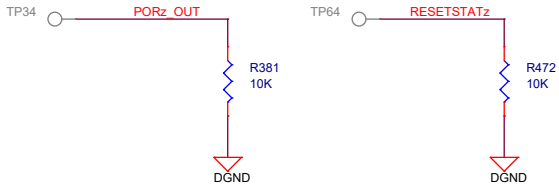
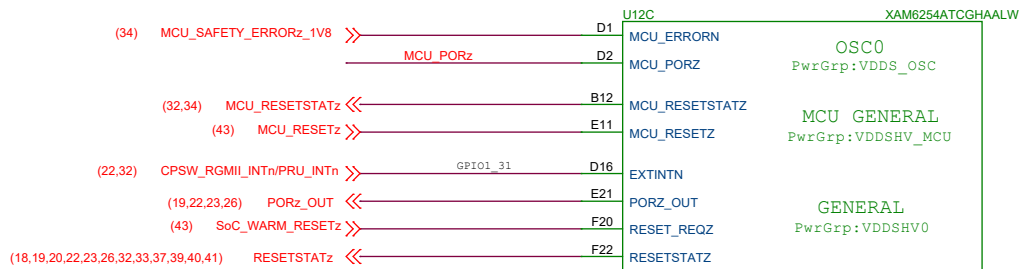
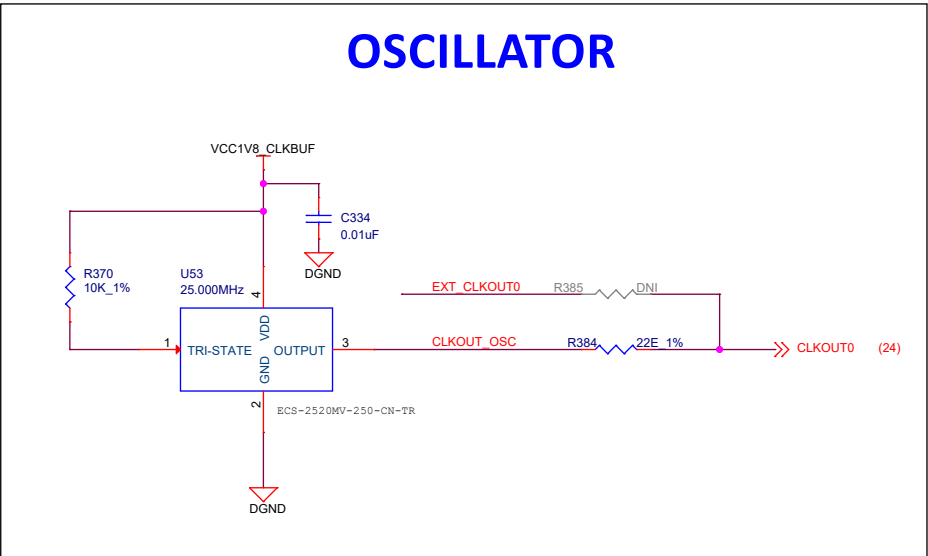
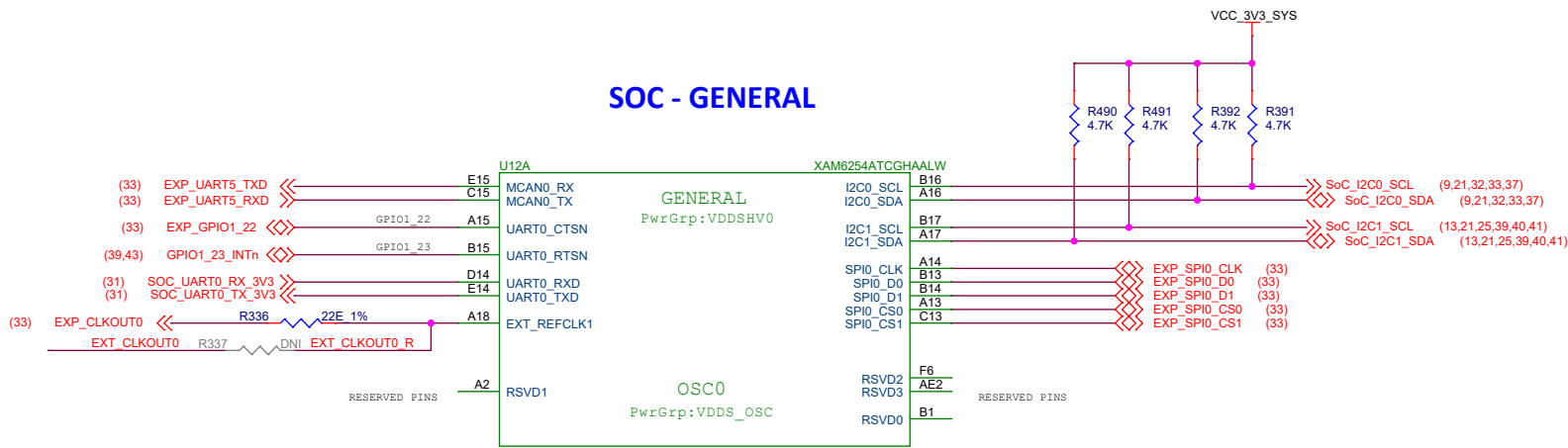
HDMI INTERFACE

U12N

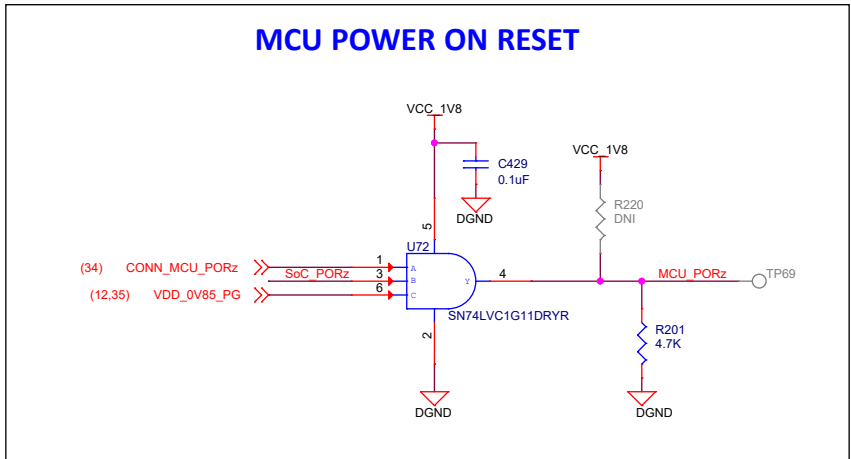
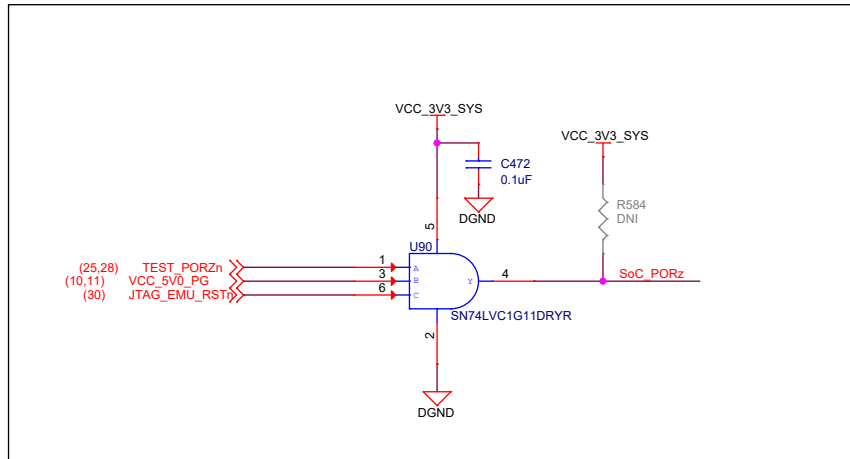
XAM6254ATCGHAALW

VOUT0_DATA0	U22	SoC VOUT0_DATA0
VOUT0_DATA1	V24	SoC VOUT0_DATA1
VOUT0_DATA2	W25	SoC VOUT0_DATA2
VOUT0_DATA3	W24	SoC VOUT0_DATA3
VOUT0_DATA4	Y25	SoC VOUT0_DATA4
VOUT0_DATA5	Y24	SoC VOUT0_DATA5
VOUT0_DATA6	Y23	SoC VOUT0_DATA6
VOUT0_DATA7	AA25	SoC VOUT0_DATA7
VOUT0_DATA8	V21	SoC VOUT0_DATA8
VOUT0_DATA9	W21	SoC VOUT0_DATA9
VOUT0_DATA10	V20	SoC VOUT0_DATA10
VOUT0_DATA11	AA23	SoC VOUT0_DATA11
VOUT0_DATA12	AB25	SoC VOUT0_DATA12
VOUT0_DATA13	AA24	SoC VOUT0_DATA13
VOUT0_DATA14	Y22	SoC VOUT0_DATA14
VOUT0_DATA15	AA21	SoC VOUT0_DATA15
VOUT0_PCLK	AC24	SoC VOUT0_PCLK R60 0E HDMI_PCLK
VOUT0_DE	Y20	SoC VOUT0_DE
VOUT0_VSYNC	AC25	SoC VOUT0_VSYNC
VOUT0_HSYNC	AB24	SoC VOUT0_HSYNC





Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up sequence



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Title OSCILLATOR

Size PROC114A(002)

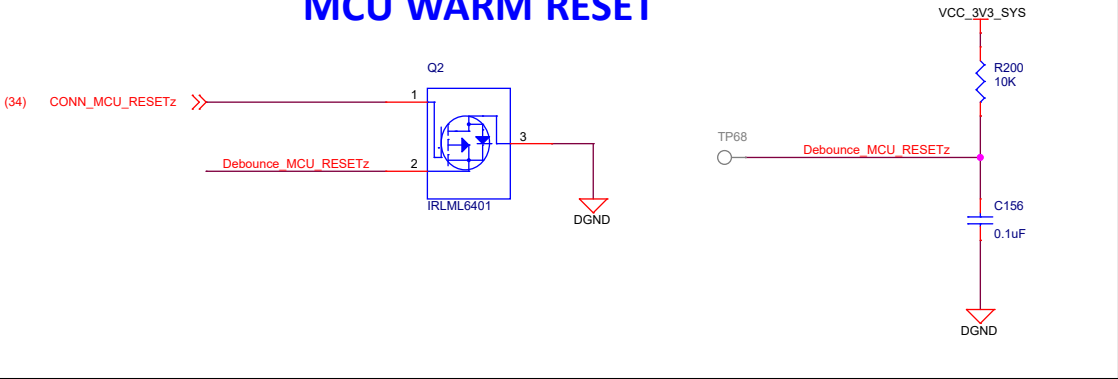
Rev

Date: Monday, December 05, 2022

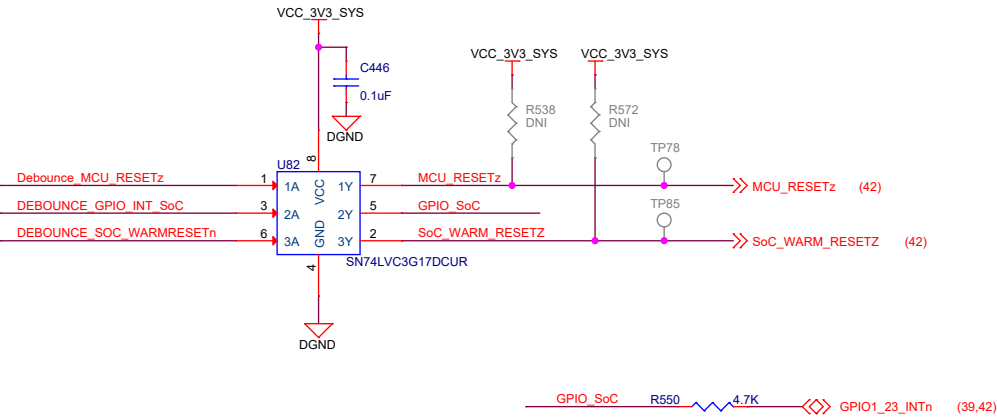
Sheet 42 of 44

RESET

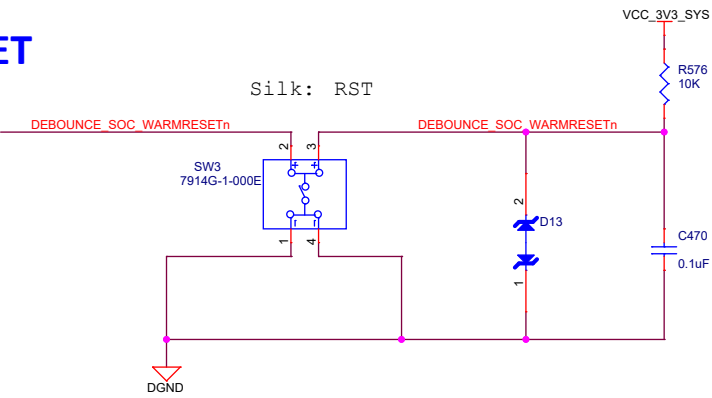
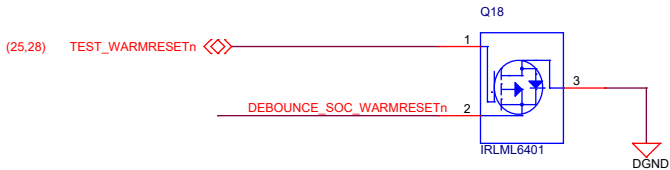
MCU WARM RESET



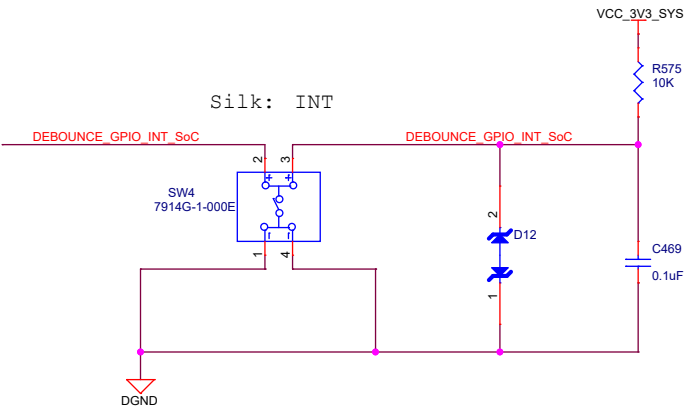
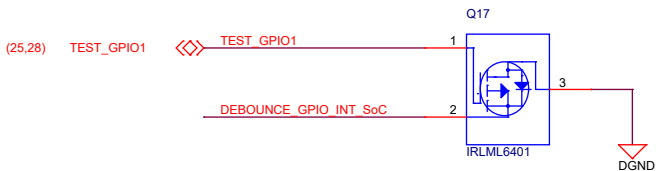
DEBOUNCE CIRCUIT



SOC WARM RESET



USER INTERRUPT



HARDWARE SCHEMATICS

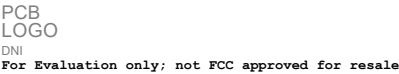
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



LABELS

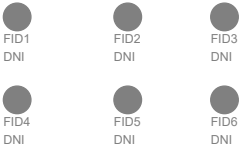
Board Serial No.



Assembly Revision



FIDUCIALS



ORDERABLE PART NO



Oderable Part Number	
Variant	Label Text
001	SK-AM62
002	SK-AM62B

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Title HARDWARE SCHEMATICS

Size PROC114A(002)

Rev

A

Date: Monday, December 05, 2022

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