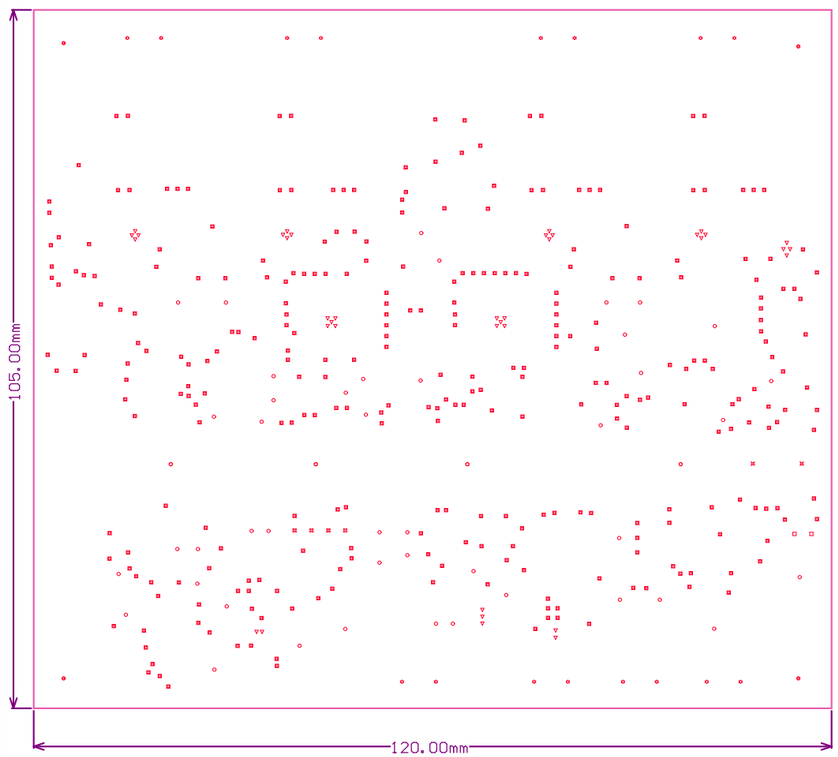

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	20.00mil	4.2	
5	GND	Copper	1.40mil		
6	Dielectric2	FR-4 High Tg	17.00mil	4.8	
7	PWR	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	20.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair
▽	37	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer
◘	304	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer
⊠	4	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer
○	44	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer
□	2	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer
✡	16	49.21mil (1.250mm)	PTH	Round	Top Layer - Bottom Layer
◉	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer
⌘	2	20.00mil (0.508mm)	NPTH	Slot	Top Layer - Bottom Layer
✪	4	60.00mil (1.524mm)	NPTH	Slot	Top Layer - Bottom Layer
	417 Total				

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Drill tolarence:
For 7.87 mil vias+0/-7.87mil
For 12 mil vias+0/-12mil
For PTH +/-3mil
For NPTH +/-2mil

ALL VIAS ARE TENTED EXCEPT THERMAL VIAS
THIS IS NOT AN IMPEDENCE CONTROLLED BOARD

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 5.90 MIL EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 63 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[ ] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-00420_BIM_ADS7128
DESIGNED FOR: PUBLIC RELEASE
FILE NAME: TIDA-00420_BIM_ADS7128.PcbDoc
ENGINEER: SREENIVASA KALLIKUPPA
LAYOUT BY: Avinash N
SCALE: 1.12
ALTIUM DESIGNER VERSION: 18.1.9.240

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00420_BIM_ADS7128	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Drill Drawing	TID #: 00420		
PLOT NAME = Fabrication Drawing	GENERATED : 3/8/2021 4:02:48 PM	TEXAS INSTRUMENTS	

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