Application Report
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Upgrading from the ADS7804/05 to the ADS8504/05 Devices

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ABSTRACT

The information contained in this document is used for current applications running with the ADS7804 or ADS7805 using the surface mount (DW) package. This document is intended as a guide to users of the ADS7804/05 devices with regards to potential compatibility issues when upgrading to the new ADS8504 and ADS8505 series of devices.

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1 Package and Pin Compatibility

The ADS8504 and ADS8505 were designed to be fully pin-compatible with the surface mount SO-28 (DW package) ADS7804 and ADS7805 devices. The updated chips feature greater throughput (up to 250 Ksps), lower power and better ac and dc performance.

The following table is hyperlinked to provide access to the associated data sheets of both the ADS78xx and ADS85xx devices.

Current ADS78xx Family	New ADS85xx Family
ADS7804 – SBAS019	ADS8504 –SLAS434
ADS7805 – SBAS020	ADS8505 – SLAS180

2 Electrical Differences

The following section describes potential electrical compatibility issues.

2.1 Absolute MAX Voltage Input Changes

The new ADS8504 and ADS8505 devices differ in the MAXIMUM working voltage. These items are presented below:

ADS7804/05 MAX Voltage Specification	
V_{ANA}	7 V
V_{DIG}	7 V
ADS8504/05 MAX Voltage Specification	
V_{ANA}	6 V
V_{DIG}	6 V

2.2 Input Impedance and Capacitance Changes

The new ADS8504 and ADS8505 devices have different input impedance and capacitance features. The major differences are noted in the table below.

PARAMETER	CONDITIONS (See the Device Data Sheet)	78 SERIES			85 SERIES			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ADSxx04								
Impedance			23			11.5		kΩ
Capacitance			35			50		pF
ADSxx05								
Impedance			23			11.5		kΩ
Capacitance			35			50		pF

2.3 Performance Compatibility

The new ADS8504 and ADS8505 devices have performance characteristics that meet or exceed the *B grade* specifications listed in the ADS7804 and ADS7805 device data sheets. Primary interest regarding specific improvements will be dependent on the actual application. In ac applications for example, the spurious-free dynamic range (SFDR) has improvements of up to 16 dB (typical).

For applications where dc performance is critical, integral non-linearity (INL) and differential non-linearity (DNL) have been improved by nearly 50%.

3 Function and Timing Differences

The following sections discuss the functionality and timing differences between the ADS7804/05 and the ADS8504/05.

3.1 Functional Compatibility

The ADS8504 and ADS8505 devices retain the same basic functionality of the ADS7804 and ADS7805 with one main exception. The ADS8504 and ADS8505 devices feature a method to abort the conversion in process. This new feature is a successive approximation register (SAR) reset option. In the ADS7804 and ADS7805 design, transitions on the R/C line were ignored while $\overline{\text{BUSY}}$ is low.

The new SAR reset feature allows the user to abort a conversion in process by taking R/C low for 40 nS (MIN) while BUSY is low. A new conversion sequence can be started after the ADC has had enough time to acquire a new sample. Figure 1 shows SAR Reset from power up.

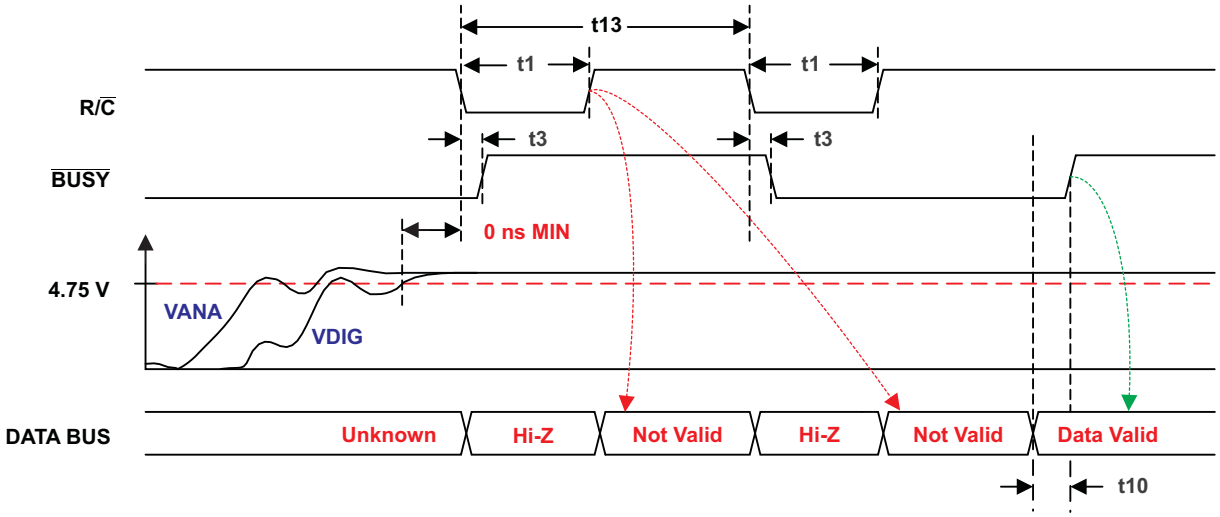

Figure 1. ADS8504/05 NEW SAR Reset Function

For designs which do not routinely monitor the status of the ADC $\overline{\text{BUSY}}$ signal, it is recommended that the host processor add a *dummy cycle* after power up as part of a device initialization sequence to ensure the new ADS8504 and ADS8505 are properly reset and ready to take formal conversion commands. This is not a requirement of the new ADS8504 or ADS8505 device, it is simply an application recommendation.

Note: in the ADS85xx series of devices, it is still required that V_{ANA} be $\leq V_{DIG}$.

3.2 Timing Compatibility

There are a number of timing changes related to the ADS8504 and ADS8505 devices that are discussed in detail throughout the following section. Depending on the specific application, these timing changes may affect the *drop in replacement* or ease of use in designs or end systems currently using the ADS7804 or ADS7805. A careful review of the following table will highlight the timing differences between the ADS7804/05 and ADS8504/05.

3.3 Comparison of the ADS7804/05 and ADS8504/05 Timing Characteristics

The following table provides a side by side comparison of the timing differences between the ADS7804/05 and the ADS8504/05. The **bold** items show the timing differences which are most likely to have an impact on current ADS7804/05 designs when upgrading to the ADS8504/05.

SYMBOL	DESCRIPTION	ADS7804			ADS8504			UNIT
ADS7804 / ADS8504		MIN	TYP	MAX	MIN	TYP	MAX	
t1 / t_{w1}	**Convert Pulse Width**	**40**		**6000**	**40**		**1750**	nS
t2 / t_a	**Data Valid Delay after R/C LOW**			**8**		2.2	**3.2**	µs
t3 / t_{pd}	**BUSY Delay from R/C LOW**			**65**		15	**25**	nS
t4 / t_{w2}	**BUSY LOW**			**8**			**2.2**	µs
t5 / t_{d1}	BUSY Delay after End of Conversion		220			5		ns
t6 / t_{d2}	Aperture Delay		40			5		ns
t7 / t_{conv}	**Conversion Time**		7.6	**8**			**2.2**	µs
t8 / t_{acq}	Acquisition Time	2			1.8			µs
t9 / t_{dis}	Bus Relinquish Time	10	35	83	10	30	83	ns
t10 / t_{d3}	**BUSY Delay after Data Valid**	**50**	**200**		**35**	**50**		ns
t11 / t_v	**Previous Data Valid after R/C LOW**		**7.4**		**1.5**	**2**		µs
t7 + t8 / t_{conv} + t_{acq}	Throughput Time		9	10			4	µs
t12 / t_{su}	R/C to C/S Setup Time	10			10			nS
t13 / t_c	Time Between Conversion	10			4			µs
t14 / t_{en}	Bus Access Time and BYTE Delay	10		83	10	30	83	ns

SYMBOL	DESCRIPTION	ADS7805			ADS8505			UNIT
AD7805 / ADS8505		MIN	TYP	MAX	MIN	TYP	MAX	
t1 / t_{w1}	**Convert Pulse Width**	**40**		**7000**	**40**		**1750**	nS
t2 / t_a	**Data Valid Delay after R/C LOW**			**8**		2.2	**3.2**	µs
t3 / t_{pd}	**BUSY Delay from R/C LOW**			**65**			**25**	nS
t4 / t_{w2}	**BUSY LOW**			**8**			**2.2**	µs
t5 / t_{d1}	BUSY Delay after End of Conversion		220			5		ns
t6 / t_{d2}	Aperture Delay		40			5		ns
t7 / t_{conv}	**Conversion Time**		7.6	**8**			**2.2**	µs
t8 / t_{acq}	Acquisition Time	2			1.8			µs
t9 / t_{dis}	Bus Relinquish Time	10	35	83	10	30	83	ns
t10 / t_{d3}	**BUSY Delay after Data Valid**	**50**	200		**35**	50		ns
t11 / t_v	**Previous Data Valid after R/C LOW**		**7.4**		1.5	**2**		µs
t7 + t8 / t_{conv} + t_{acq}	Throughput Time		9	10			4	µs
t12 / t_{su}	R/C to C/S Setup Time	10			10			nS
t13 / t_c	Time Between Conversion	10			4			µs
t14 / t_{en}	Bus Access Time and BYTE Delay	10		83	10	30	83	ns

4 Potential Application Issues

The conversion speed of the ADS8504 and ADS8505 devices has been increased to 250 KSPS and the convert signal pulse duration has decreased from a maximum of 6-7 μS (depending on the converter) to 1.75 μS . This presents two potential application issues depending on the applied R/C input strobe. Throughout the following discussion, remember that the Read/Convert signal activates the output data when the signal is HIGH, and starts a conversion cycle when the signal goes LOW.

4.1 R/C Signal Timing

Customers using the ADS7804/05 devices with a 5 μS convert start pulse, or fixed 50:50 duty cycle clock at 100 kHz applied to the R/C input will see the $\overline{\text{BUSY}}$ signal return high before the R/C strobe returns high. In the ADS8504 and ADS8505 devices, the conversion cycle is complete nearly 4 times faster than the ADS7804 and ADS7805 devices. If the $\overline{\text{BUSY}}$ output from the ADC is used to trigger an interrupt service routine, delays must be added to the routine to ensure the R/C pulse has returned high before attempting to read the conversion results. Attempting to read the DATA bus while R/C is low (data bus is HI-Z) will produce indiscriminate results.

4.2 Using the $\overline{\text{BUSY}}$ Signal as a Write Strobe

The $\overline{\text{BUSY}}$ signal can be used as a means to strobe conversion data into the host processor, provided that the R/C input has been taken to a high state prior to completion of the conversion. The ADS8504 and ADS8505 will release $\overline{\text{BUSY}}$ approximately 2 μS after the application of the low going edge of R/C. In the ADS7804 and ADS7805 device, the $\overline{\text{BUSY}}$ signal is released approximately 8 μS after the application of R/C. The user must, therefore, ensure all background tasks are complete and the host processor is ready to receive data within 1.8 μS, or risk losing the conversion results.

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