Application Report
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TPS54620 Parallel Operation

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ABSTRACT

The TPS54620 is a synchronous, step-down, dc-dc converter with integrated high- and low-side FETs. It is rated for a continuous output of 6 A. In order to increase the output current capability, it is possible to operate two TPS54620 circuits in parallel. Certain techniques are required in the design to ensure that each of the TPS54620 converters provides an equal share of the output current. This application report details the design, operation, and performance of a parallel TPS54620 dc/dc converter.

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1 Introduction

The TPS54620 is a 17-V input, 6-A output, synchronous, step-down switcher with integrated FET (SWIFT™ converter). To increase the output current above the rated 6 A, it is possible to connect two TPS54620 converters in parallel. This configuration allows both integrated circuits to share output current equally, and the total maximum output current is 6 A + 6 A = 12 A. However, practical difficulties exist when two such supplies are connected in parallel, and they may not share current equally. If properly designed, these difficulties can be overcome so that a functional stable circuit is possible.

2 Control Types

Current-mode control is usually required when designing parallel converters. To see why current-mode control is important, it is first necessary to understand some basic differences between current-mode and voltage-mode control. For this application report, the pin name conventions for the TPS54620 are used as shown in the Figure 5 schematic.

2.1 Voltage-Mode Control

A simplified voltage-mode control block diagram is shown in Figure 1. In voltage-mode control, only one feedback loop is present in the control circuitry. A portion of the output voltage is fed back to the error amplifier (V_SNS) by the divider network of Z1 and Z2 and compared to a voltage reference. The output of the error amplifier (COMP) is compared to a PWM ramp voltage waveform. The voltage mode control waveforms are shown in Figure 2. While the PWM ramp voltage is below the output of the error amplifier, the high-side switch element is ON and the output of the converter at the switching node (PH) is approximately equal to Vin. When the PWM ramp voltage exceeds the error amplifier output, the high-side switch element is turned OFF, and the switching node output voltage is approximately 0 V. The output waveform at the switching node is a pulse train that switches from Vin to ground with a duty cycle of D. The output inductor and capacitor comprise a second-order filter that passes the dc component of the pulse train. In this way, the output voltage is regulated to the average value of the switching node voltage, Vout = D × Vin, where D is the duty cycle of the converter. The output current has no direct control. Any change in the load current causes a corresponding change in the output voltage. In the example waveforms, a step load change causes the output voltage to decrease. The error amplifier output voltage rises in response and causes the PWM duty cycle to increase temporarily to allow the inductor current to ramp up to the new required load current. When the desired load current is achieved, the control loop responds and the error amplifier output voltage returns to the previous level and the PWM duty cycle returns to the value required for proper voltage regulation. Because the switch current has no direct control, it is difficult to implement current sharing with voltage-mode control.

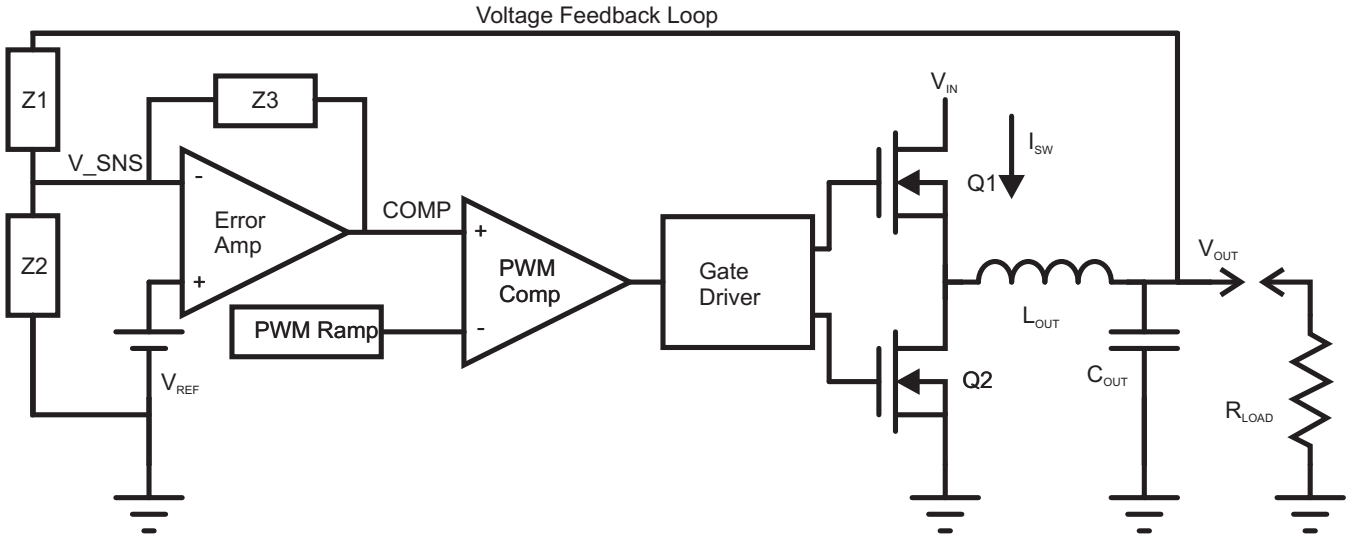

Figure 1. Voltage-Mode Control Block Diagram

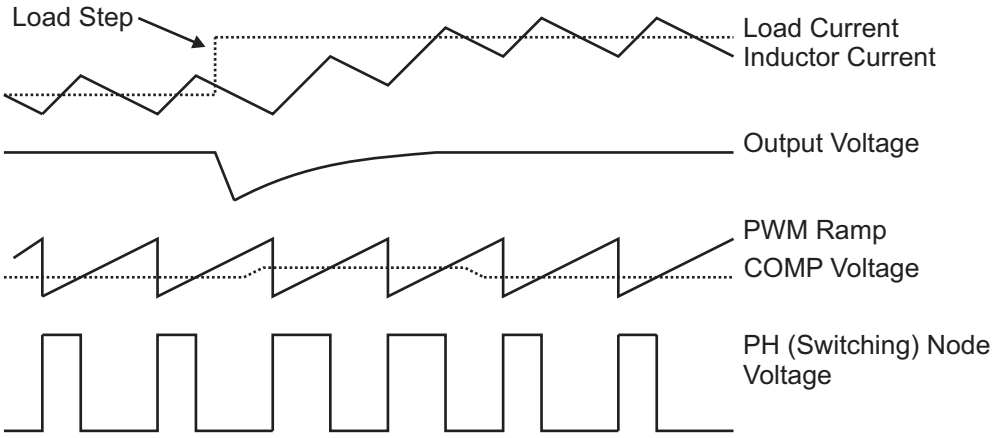

Figure 2. Voltage-Mode Control Waveforms

2.2 Peak Current-Mode Control

A simplified peak current-mode control block diagram is shown in Figure 3. Peak current-mode control uses two feedback loops: an inner current-sense loop and an outer voltage-sense loop. As in voltage-mode control, a portion of the output voltage is fed back to the error amplifier by the divider of Z1 and Z2 and compared to an internal reference. Other than that, the control scheme differs substantially. The peak current-mode control waveforms are shown in Figure 4. The output of the error amplifier at the COMP pin is a voltage that is proportional to the required peak switch current. The peak switch current to COMP pin voltage characteristic is specified by the transconductance of the power stage, gm_{COMP}, that converts the COMP voltage to a reference current. In the inner current control loop, this reference current is compared to the switch current. The switch current consists of the ac inductor current superimposed over the output load current. This ac inductor current has the characteristic shape of a ramp and serves as the equivalent to the PWM ramp in voltage-mode control. For any given cycle, when the peak switch current is equal to the reference current, the high-side switch is turned off, setting the duty cycle for the converter. When a change in output current is required, the fed-back voltage at V_SNS changes and the COMP pin voltage increases if more current is required and decreases if less current is required. In the example waveforms, a step load change causes the output voltage to decrease. The COMP pin voltage rises in response and allows a higher peak switch current for the ensuing switching cycles. When the peak current is increasing in sequential switching cycles, the PWM duty cycle increases as well. The resultant change in duty cycle allows the inductor current to ramp up or down as required, setting a new steady-state load current. The COMP pin voltage remains at the new level as it directly controls the output current.

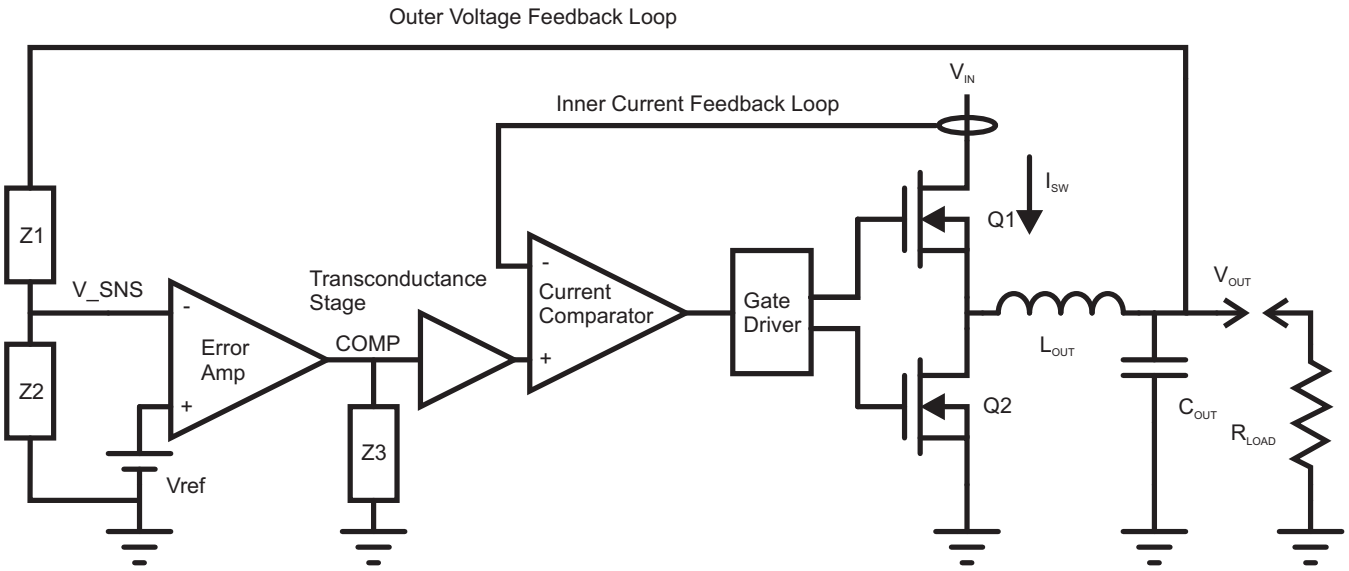

Figure 3. Peak Current-Mode Control Block Diagram

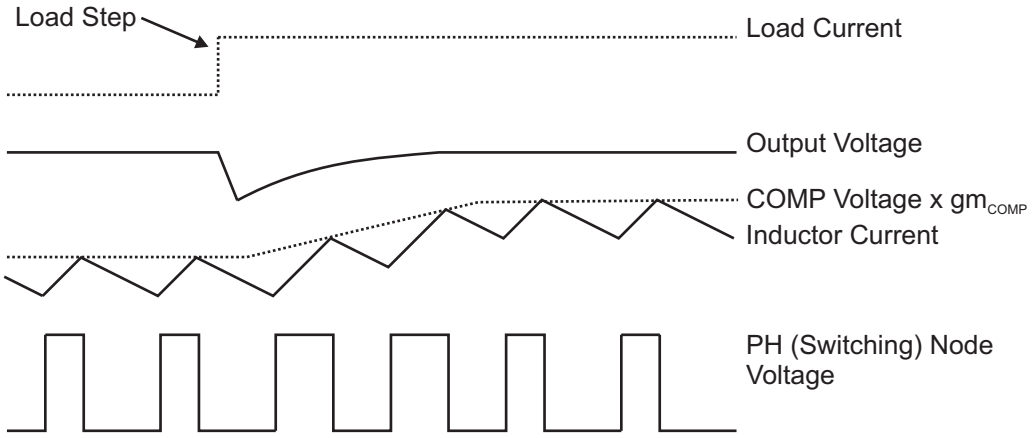

Figure 4. Peak Current-Mode Control Waveforms

So, for peak current-mode control, the output current is proportional to the COMP pin voltage. This provides a convenient method to allow current sharing. If the COMP pin voltage of two converters in parallel are connected together and the power stage transconductance of each are closely matched, then the two parallel converters each contribute an equal amount of load current.

3 Parallel Operation

A few considerations need to be made to operate the TPS54620 converters in parallel. As previously explained, it is necessary to ensure that the COMP pin voltage of both devices is common. The easiest way to achieve this is by connecting the two COMP pins together. Because a single regulated output is desired, the fed-back portion of the output at V_SNS must be the same for both devices. Use a single-voltage, set-point divider network, and connect the V_SNS pins together to accomplish this. The devices must operate at a common frequency with a synchronous clock. It is preferable to use an external clock source driving the RT/SYNC pin. Driving one device out of phase with the other reduces the ripple on the input voltage supply; so, an inverter is used to produce an out-of-phase clock circuit from the external clock source. Both the devices must start up at the same time. Hence, the SS/TR pins of both devices are connected together. The V_SNS pins also are tied up together to maintain the same error voltage in both the devices.

4 Design Procedure

For parallel operation, the general TPS54620 design steps can be followed. An example design is shown in the Figure 5 schematic. The important design steps are detailed as follows.

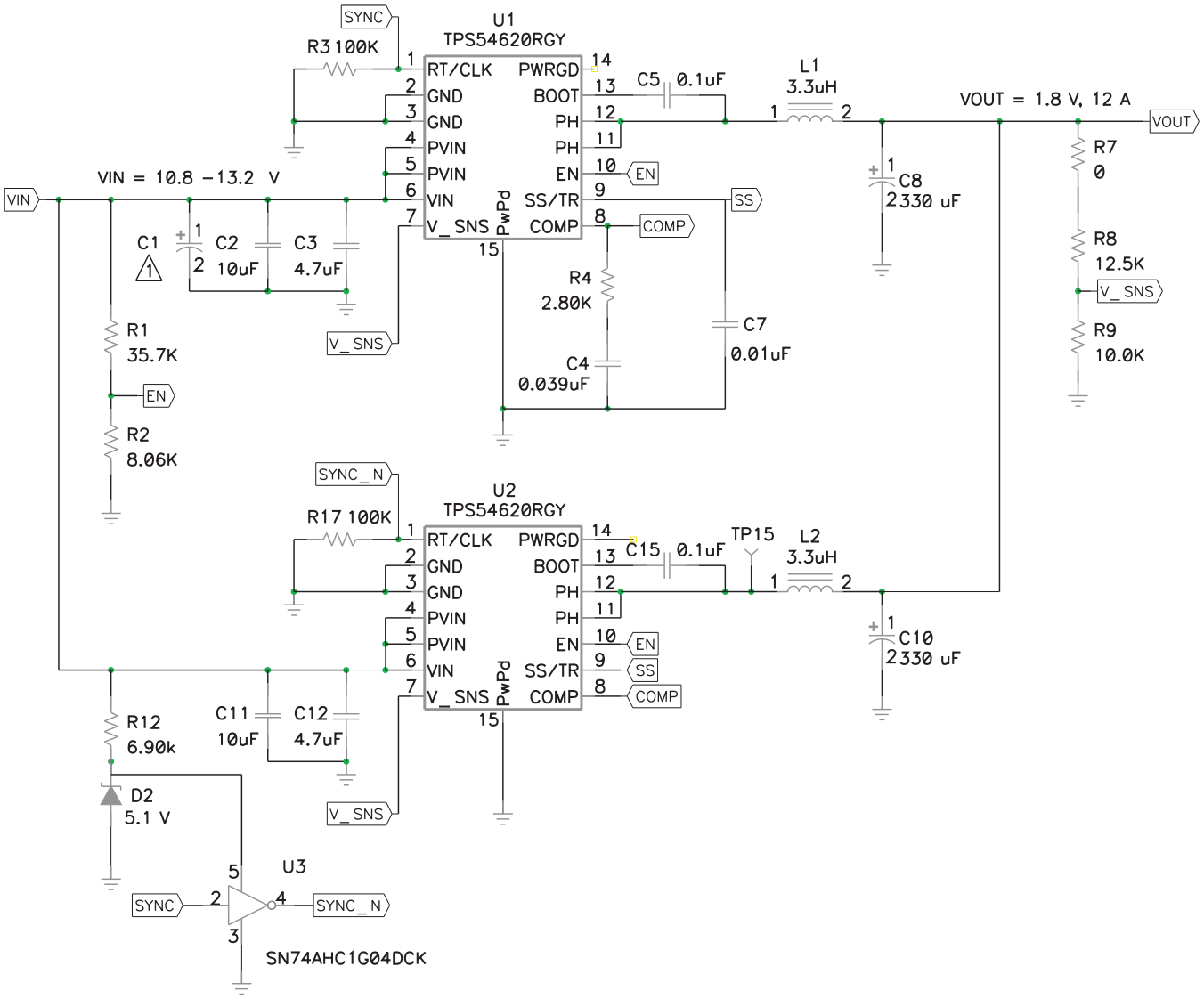

Figure 5. TPS54620 Example Design

4.1 Design Requirements

The design requirements for this example are provided in Table 1.

Table 1. Design Requirements

Parameter	Value
Output Voltage	1.8 V
Output Current	12 A
Input Voltage	12 V +/- 10%
Transient Response, 6-A load step	50 mV
Switching Frequency	480 kHz

4.2 Operating Frequency

The first step is to select a switching frequency for the regulator. The tradeoff between higher and lower switching frequencies must be considered. Higher switching frequencies may produce a smaller solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which adversely affect the converter's efficiency and thermal performance. In this design, a moderate switching frequency of 400 kHz is selected to achieve both a small solution size and a high-efficiency operation. When operating the TPS54620 in parallel, it is important to keep the two converters synchronized. The two TPS54620 devices are operated using an externally supplied clock. The external clock is used to drive the U1 converter's RT/CLK pin directly. An inverter is used to derive an additional clock signal 180° out of phase with the external clock. This inverted clock is used to drive the U2 converter. Operating the two converters out of phase reduces the input voltage ripple. The RT/CLK pin of each converter is terminated with an RT timing resistor set for the nominal 400-kHz operating frequency. The required resistor value can be calculated using Equation 1.

$$\mathrm{Rrt(k\Omega)} = 48000 \cdot \mathrm{Fsw\,(kHz)}^{-0.997} - 2 \tag{1}$$

4.3 Output Voltage Set Point

The resistor divider network R8 and R9 is used to set the output voltage. For the example design, 10 kΩ was selected for R9. Using Equation 2, R8 is calculated as 12.5 kΩ.

$$R8 = \frac{R9 \cdot (Vout - Vref)}{Vref} \tag{2}$$

4.4 Output Inductor Selection

This parallel design uses two output inductors, L1 and L2. Each inductor must be selected to handle one-half of the total output current; thus, the selection criteria is the same as for a single output design. To calculate the value of the output inductor, use Equation 3. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Although the inductor ripple value is generally at the discretion of the designer, KIND is normally from 0.1 to 0.3 for the majority of applications.

$$\mathrm{L1} = \frac{\mathrm{Vinmax} - \mathrm{Vout}}{\mathrm{Io} \cdot \mathrm{Kind}} \cdot \frac{\mathrm{Vout}}{\mathrm{Vinmax} \cdot f\mathrm{sw}} \tag{3}$$

For this design example, use KIND = 0.2 and the inductor value is calculated to be 3.18 µH. For this design, a nearest standard value was chosen: 3.3 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 5 and Equation 6

$$\mathrm{Iripple} = \frac{\mathrm{Vinmax} - \mathrm{Vout}}{\mathrm{L1}} \cdot \frac{\mathrm{Vout}}{\mathrm{Vinmax} \cdot f\mathrm{sw}} \tag{4}$$

$$\mathrm{ILrms} = \sqrt{\mathrm{Io}^2 + \frac{1}{12} \cdot \left(\frac{\mathrm{V_o} \cdot (\mathrm{Vinmax} - \mathrm{Vo})}{\mathrm{Vinmax} \cdot \mathrm{L1} \cdot f\mathrm{sw}} \right)^2} \tag{5}$$

$$\mathrm{ILpeak} = \mathrm{Iout} + \frac{\mathrm{Iripple}}{2} \tag{6}$$

For this design, the RMS inductor current is 6.02 A, and the peak inductor current is 6.84 A. The chosen inductor is a Coilcraft MSS1048 series 3.3 µH. It has a saturation current rating of 7.38 A and a RMS current rating of 7.22 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated in the preceding equations. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

4.5 Input Capacitor Selection

The TPS54620 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the PVIN input voltage pins and 4.7 µF on the VIN input voltage pin. In some applications, additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. For this design, the PVIN and VIN pins are tied together to use a common input voltage supply. The U1 and U2 inputs are bypassed by a 10-µF capacitor and a 4.7-µF capacitor in parallel.

4.6 Output Capacitor Selection

With an output current capability of 12 A, it is reasonable to expect large load step transients. When the initial current step occurs, the output capacitors are required to provide the energy until the control loop can respond to increase the output of the converter. The output voltage must not fall more than 50 mV in response to a 6-A load step transient. Use Equation 7 to determine the minimum output capacitance to meet this requirement.

$$C_{OUT} > \frac{2 \cdot \Delta I_{OUT}}{F_{SW} \cdot \Delta V_{OUT}} \tag{7}$$

The required minimum capacitance is 500 µF. To meet this requirement, a 330-µF Sanyo POSCAP capacitor is used at each output for a combined capacitance of 660 µF.

4.7 Slow-Start Capacitor Selection

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large and requires large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54620 reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both these problems. The soft-start capacitor value can be calculated using Equation 8. For this circuit, both converters must start up simultaneously; so, the SS pins are tied together and a single, slow-start capacitor is used. The slow-start charge current , Iss is doubled: 2 x 2.3 µA = 4.6 µA and Vref is 0.8 V. The example circuit has the slow-start time set to an arbitrary value of 1.75 ms which requires a 10-nF capacitor.

$$\text{C7(nF)} = \frac{\text{Tss(ms)} \cdot \text{Iss}(\mu\text{A})}{\text{Vref(V)}} \tag{8}$$

4.8 Boot Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating.

4.9 Compensation Design

The compensation design is a tradeoff between stability and the load transient response. Lesser phase margin means a great transient response, but the stability of the system suffers whereas a higher phase margin degrades the transient response and improves stability. Usually, the control loop is designed for a phase margin of 60°. This provides the desired tradeoff between load transient and stability. For this design, a reasonable closed-loop crossover frequency of 25 kHz is specified. Because the COMP pins of the two devices are tied together, the compensation network needs to be common as well. Two factors must be considered when the COMP pins are tied together. The COMP pin now is driven by both transconductance amplifiers, so the gm_{ea} term is doubled. Also, the power stage transconductance is effectively doubled. For this design, Type 2B compensation is used with a single resistor and capacitor in series from COMP to ground.

The required compensation resistor R4 is given by:

$$R4 = \frac{2 \cdot \pi \cdot F_{CO} \cdot V_{OUT} \cdot C_{OUT}}{2 \cdot gm_{EA} \cdot V_{REF} \cdot 2 \cdot gm_{PS}} \tag{9}$$

And the compensation capacitor is given by

$$C4 = \frac{R_O \cdot C_{OUT}}{R4} \tag{10}$$

Where:

- F_{co} = Closed-loop crossover frequency
- V_{OUT} = Output voltage
- C_{OUT} = Output capacitance
- Gm_{EA} = Error amplifier transconductance
- V_{REF} = Reference voltage
- Gm_{PS} = Power stage transconductance

For the chosen closed-loop crossover frequency of 25 kHz, Equation 9 and Equation 10 yield:

R4 = 2803 Ω

C4 = 0.035 µF

Using standard values, C4 is 2.80 kΩ and C4 is 0.039 µF.

5 Performance

The performance of the TPS54620 parallel circuit of Figure 5 is detailed as follows. For all data, the input voltage is 12 V, the output voltage is 1.8 V, and the ambient temperature is 25° C.

5.1 Current Sharing

An important performance criterion of the parallel design is the ability to equally share current between the two converters of U1 and U2. The current-sharing performance is shown in Figure 6.

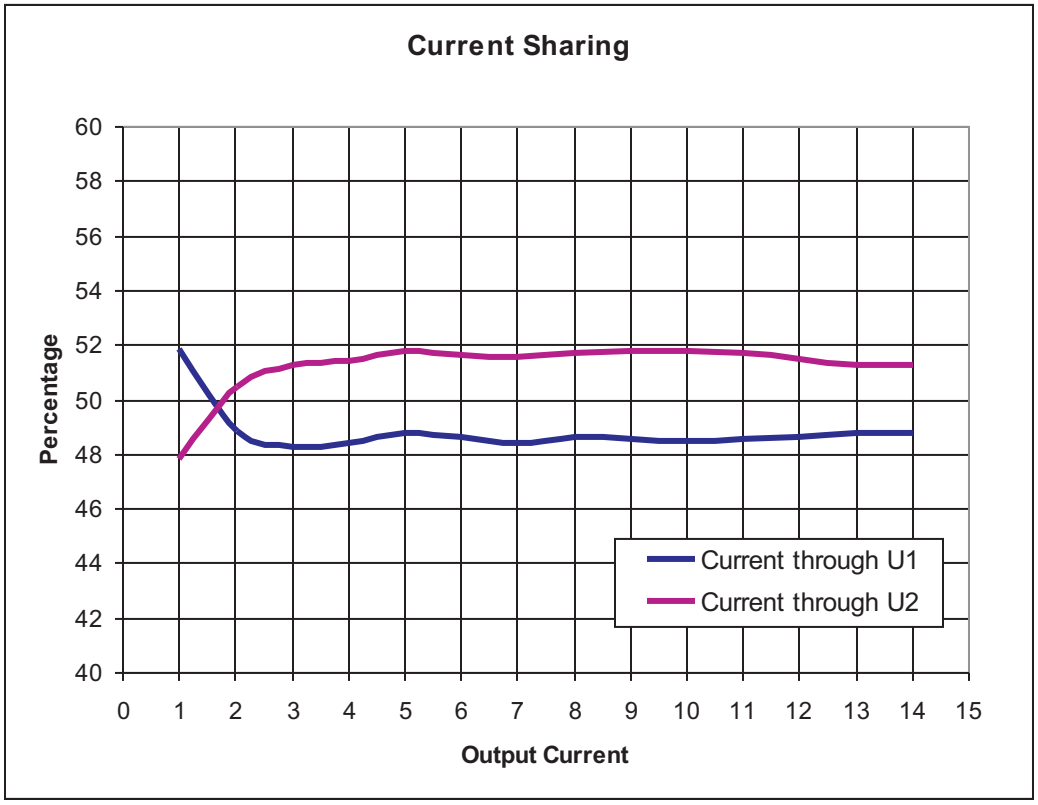

Figure 6. TPS54620 Parallel Circuit Current Sharing

5.2 Efficiency

The TPS54620 parallel circuit efficiency is shown in Figure 7.

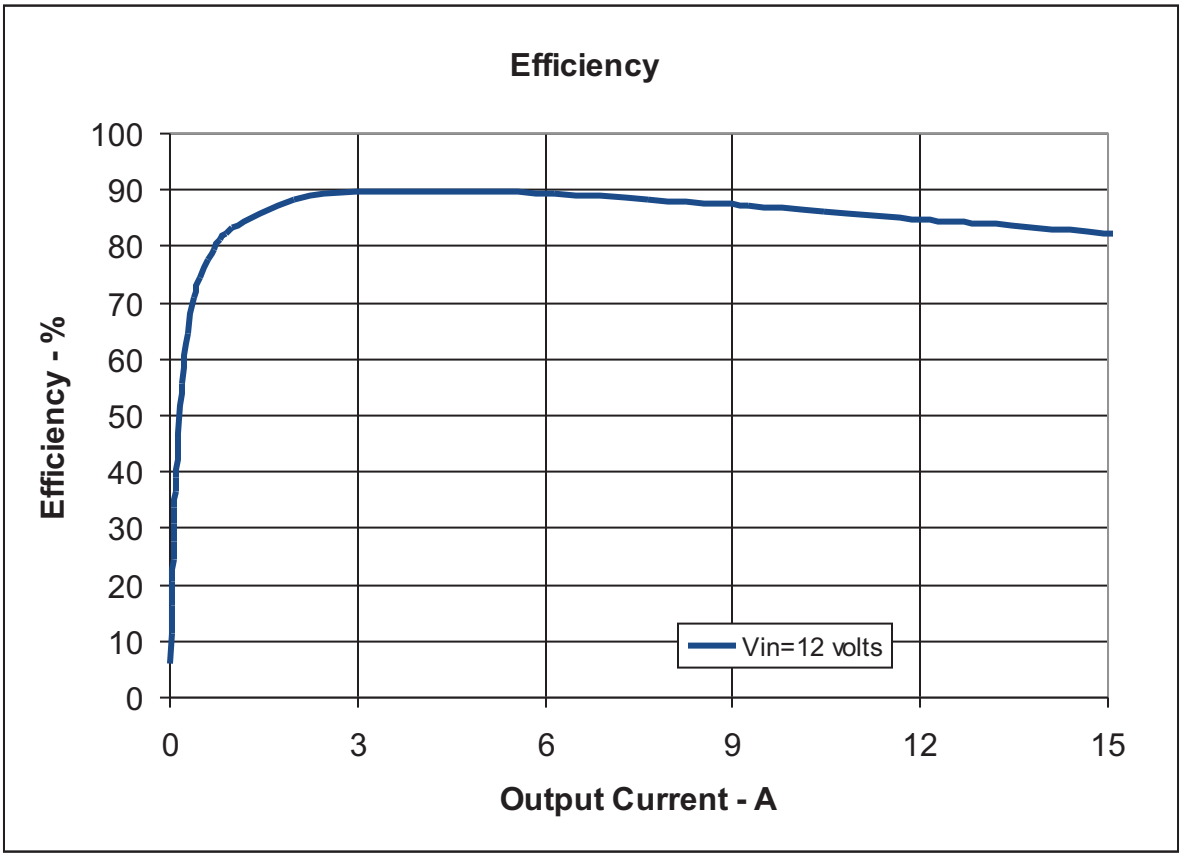

Figure 7. TPS54620 Parallel Circuit Efficiency

5.3 Output Voltage Ripple

The TPS54620 parallel circuit output voltage ripple is shown in Figure 8. The output current is 12 A.

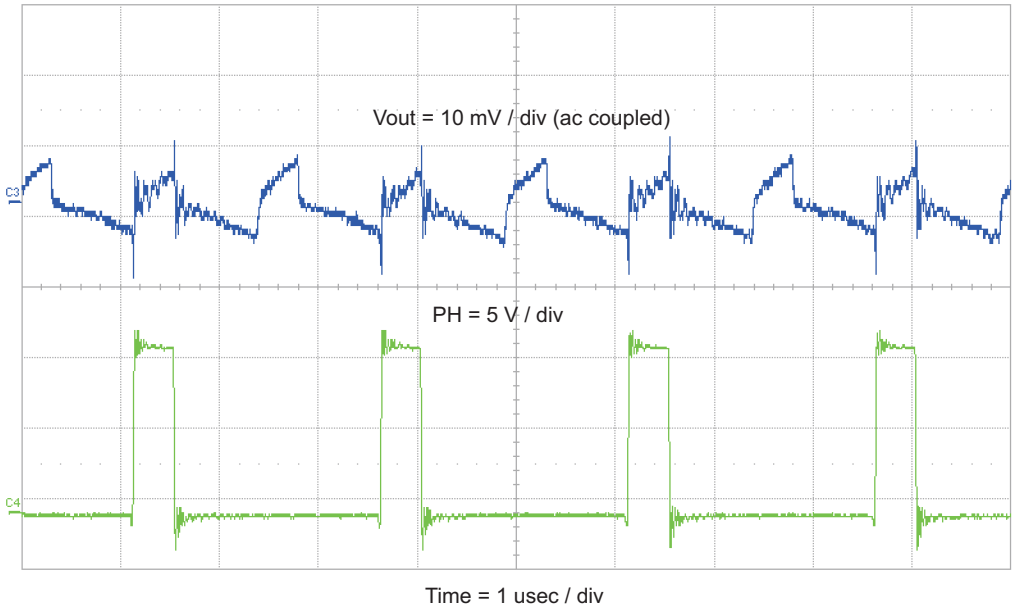

Figure 8. TPS54620 Parallel Circuit Output Voltage Ripple

5.4 Input Voltage Ripple

The TPS54620 parallel circuit input voltage ripple is shown in Figure 9. The output current is 12 A.

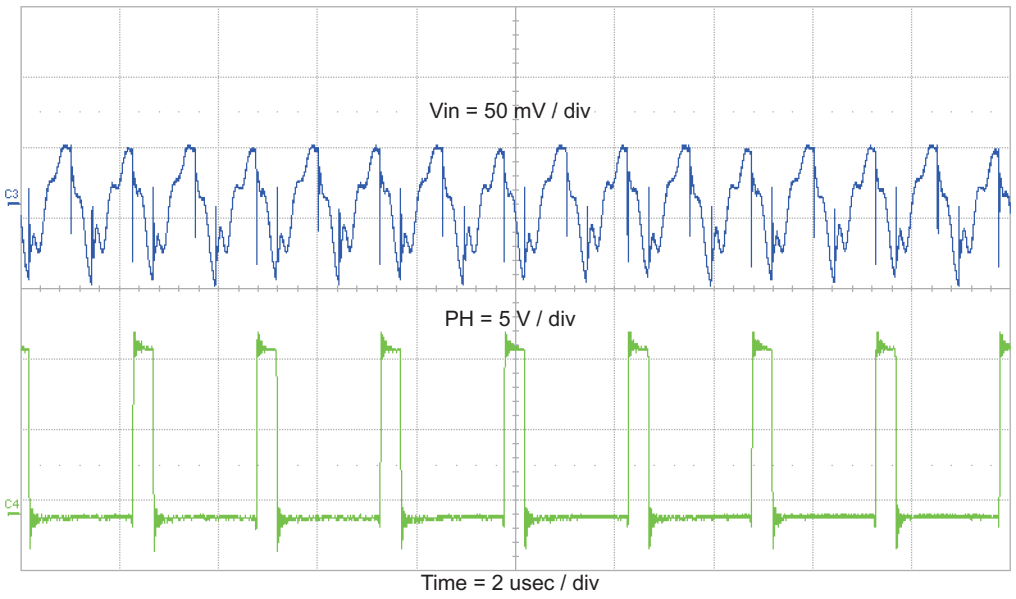

Figure 9. TPS54620 Parallel Circuit Input Voltage Ripple

5.5 Switching Node and Inductor Current Waveforms

The switching node (PH) and inductor current waveforms are shown in Figure 10. The output current is 12 A. Because the external clock signals provided to the U1 an U2 converters are out of phase, the switching node waveforms and the ac inductor currents are also out of phase. This helps to reduce input and output voltage ripple.

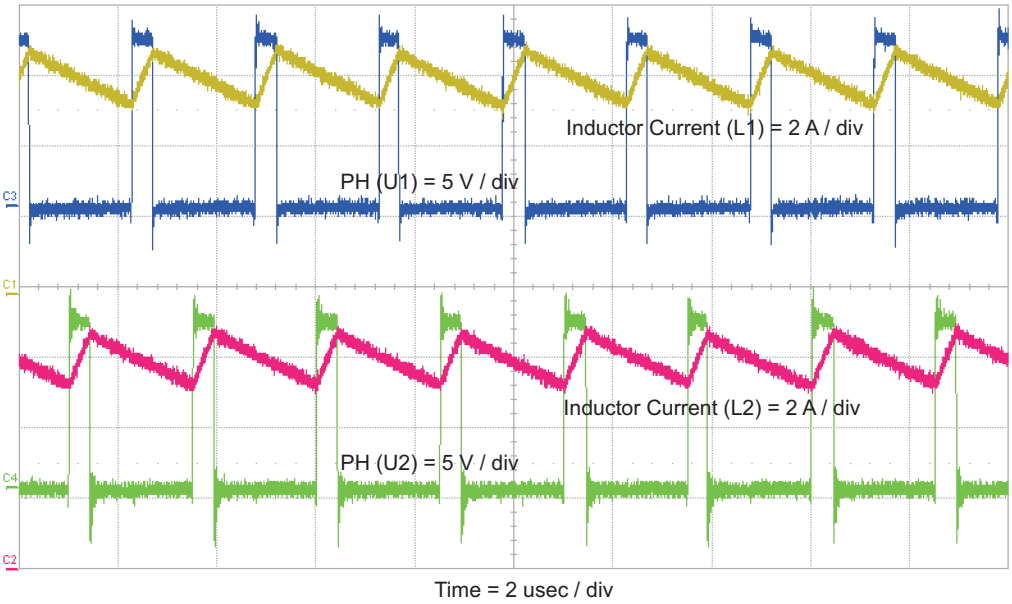

Figure 10. Switching Node and Inductor Current Waveforms

5.6 Closed-Loop Response

The closed-loop response for the parallel TPS54620 circuit is shown in Figure 11. The measured closed loop crossover frequency is 26 kHz, which is close to the intended crossover frequency of 25 kHz. The measured phase margin is 90°.

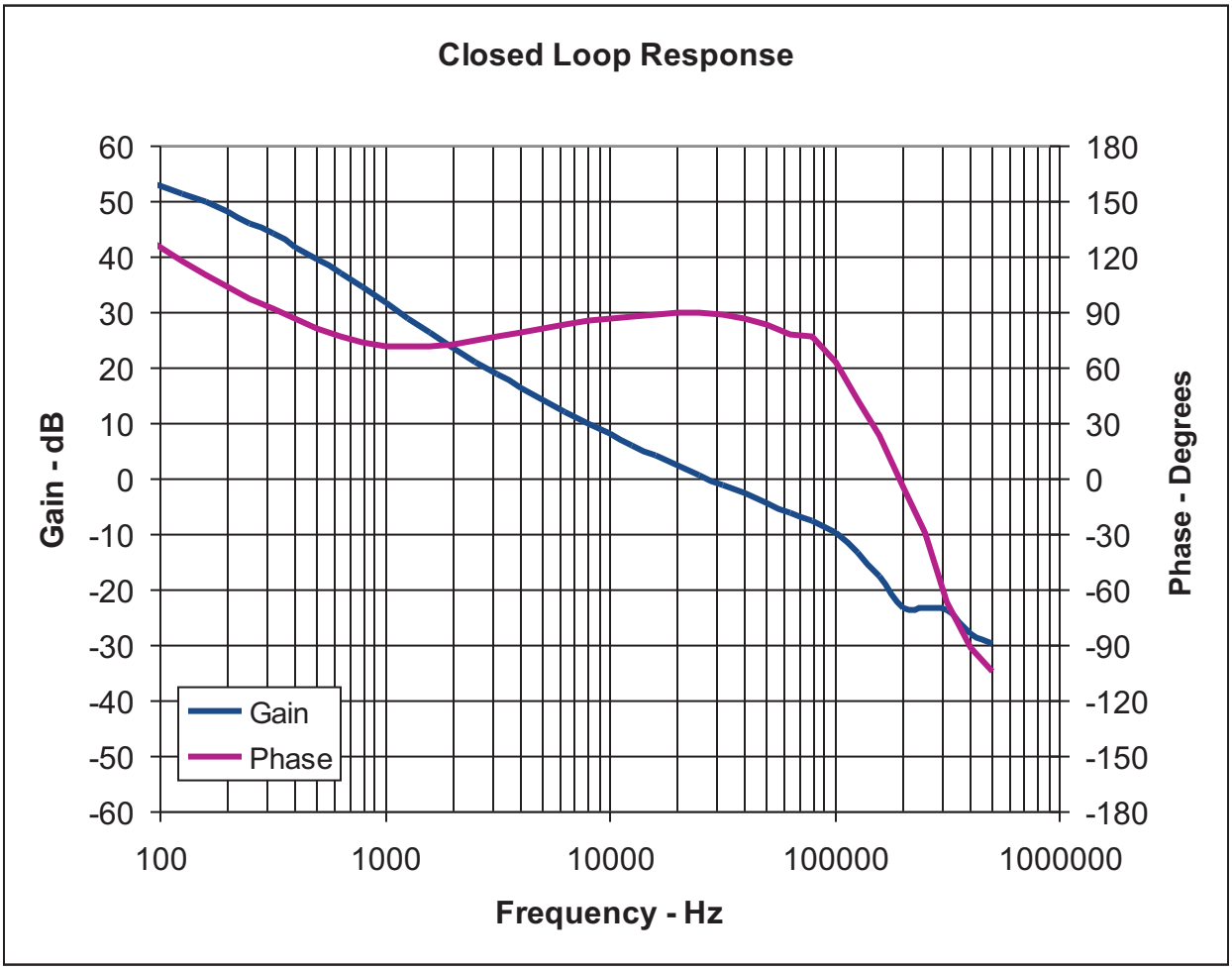

Figure 11. Closed-Loop Response

5.7 Transient Response

The parallel circuit was designed to provide good transient response. To reduce switching node waveform jitter, the closed-loop crossover frequency is limited to 25 kHz. To allow for low-voltage overshoot and undershoot during transient load steps, the circuit is designed using 2 x 330-µF special polymer output capacitors. The transient voltage change is limited to less than 50 mV for a 3-A to 9-A load step shown in Figure 12.

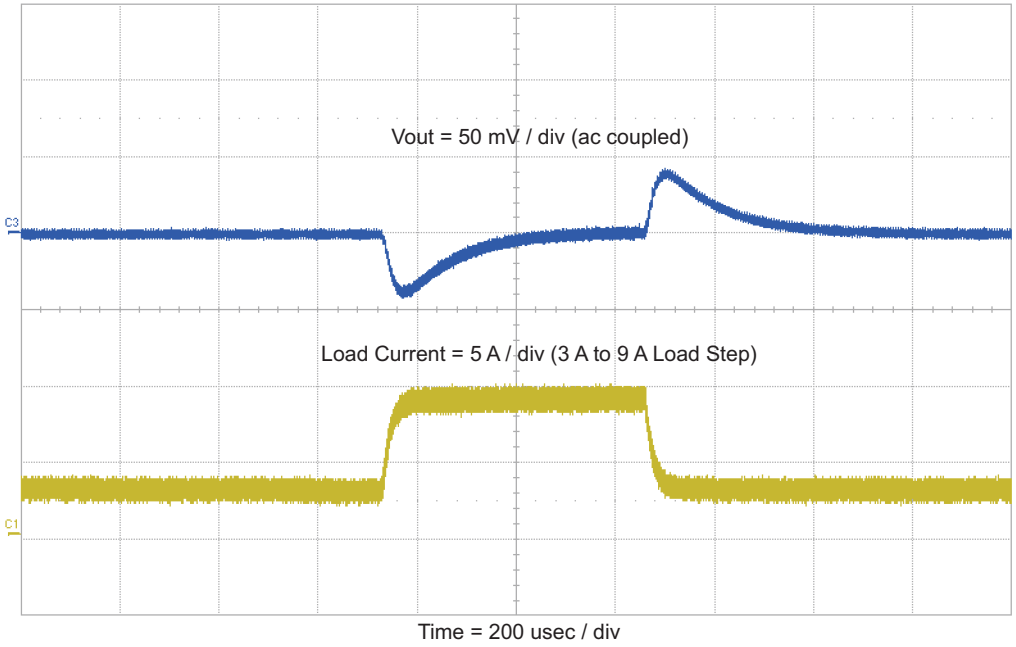

Figure 12. Transient Response

6 Conclusion

The parallel circuit using the TPS54620 performs closely to its intended design specifications. The key design parameter is the calculation of the compensation components. When the COMP pins are tied together, the effective transconductance of the error amplifier and power stage must be doubled. To keep the switching node jitter to acceptable levels, the closed-loop crossover frequency must be restricted to at or below 25 kHz. With this low, closed-loop bandwidth, it may be necessary to use a substantial amount of output capacitance if the voltage overshoot and undershoot due to transient load step changes is to be kept low. With these constants, it is possible to design a stable parallel circuit that can provide double the rated output current for the TPS54620.

The circuit demonstrated in this application report is available as PR975. For additional information, see the TPS54620 product folder on the TI Web site.

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