Clock jitter analyzed in the time domain, Part 2

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Introduction

Part 1 of this three-part article series focused on how to accurately estimate jitter from a clock source and combine it with the aperture jitter of an ADC. In this article, Part 2, that combined jitter will be used to calculate the ADC's signal-to-noise ratio (SNR), which will then be compared against actual measurements.

Measurements with filtered sampling clock

An experiment was set up to see how well the measured clock phase noise matched the clock jitter extracted from the ADC's measured SNR. As shown in Figure 11, a Texas Instruments (TI) CDCE72010 with a Toyocom 491.52-MHz VCXO was used to generate a 122.88-MHz sampling clock, and the filtered phase-noise output was measured with the E5052A from Agilent. Two different TI data converters (ADS54RF63 and ADS5483) were evaluated by using an input frequency whose SNR was predominantly limited by the sampling-clock jitter. The size of the fast Fourier transform (FFT) was chosen to be 131,000 points.

The plot in Figure 12 illustrates the measured output phase noise of the filtered CDCE72010 LVCMOS output. An FFT size of 131,000 points sets the lower integration bandwidth to ~500 Hz. The upper integration limit is set by the bandpass filter, whose effect is clearly visible in the phase-noise plot. Phase noise beyond the bandpass-filter limit shown in the plot is the noise floor of the E5052A and should not be included in the jitter calculation. The integration of the filtered phase-noise output resulted in a clock jitter of ~90 fs.

Next, a baseline for the thermal noise was established. Both ADCs were sampled with a filtered sampling clock directly from the clock-source generator with ~35 fs of jitter, and the CDCE72010 was bypassed. The input frequency was set to 10 MHz, where no impact on the SNR from clock jitter was expected. Then the aperture jitter for each ADC was determined by increasing the input frequency to where the SNR was mainly jitter-limited. Since the sampling-clock jitter is much lower than the estimated ADC aperture jitter, the calculation should be very accurate. It is also important to remember that the output amplitude of the clock

Figure 11. Test setup for correlation with filtered clock

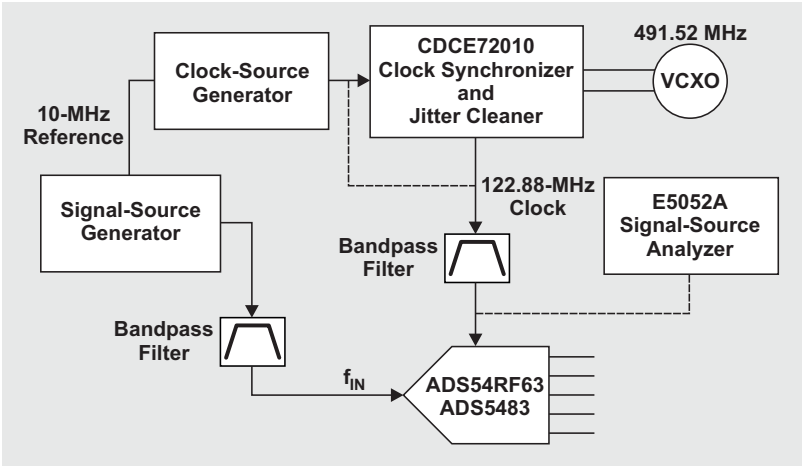
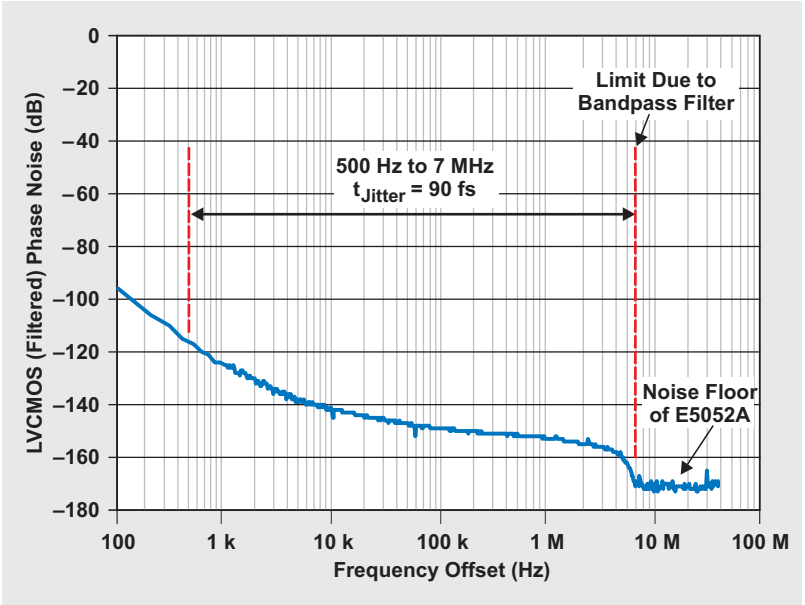


Figure 12. Measured phase noise of the filtered clock



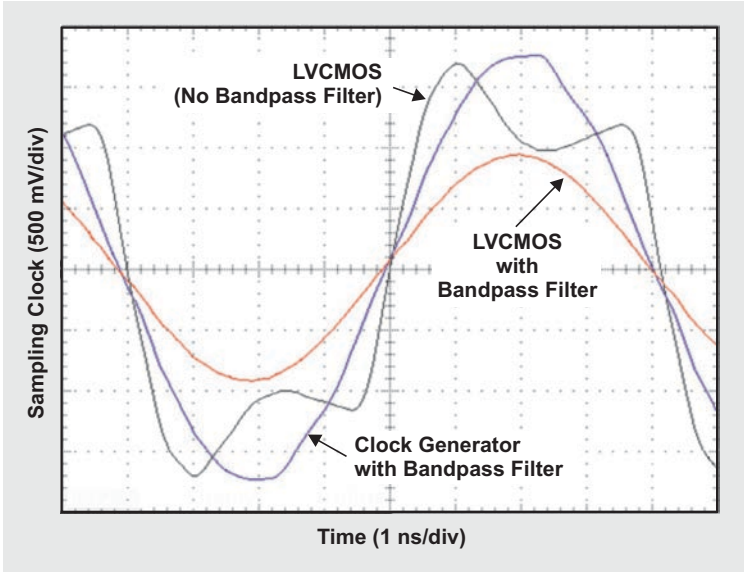
source should be increased (but not so much that it exceeds the maximum ratings of the ADC), boosting the slew rate of the clock signal until the SNR levels off.

Since it is known that the external clock jitter from the filtered output of the clock-source generator is ~35 fs, the ADC aperture jitter can be calculated by using the measured SNR results and solving Equations 1, 2, and 3 in Part 1 (Reference 1) for aperture jitter. Please see Equation 4 below. The measured SNR results as well as the calculated aperture jitter for each ADC are listed in Table 3.

With the ADC aperture jitter and the sampling-clock jitter of the CDCE72010, the ADC's SNR can be calculated and compared against the actual measurement. Using the ADC aperture jitter permits the sampling-clock jitter of the CDCE72010 to be calculated from the measured SNR values, as illustrated in Table 4. At first glance the predicted SNR values are somewhat close to the measured values. However, comparing the calculated sampling-clock jitter for the two ADCs against the measured value of 90 fs reveals a different picture. There is quite a bit of mismatch.

The reason for the mismatch is that the calculated aperture jitter is based on the fast slew rate of the clock-source generator. The bandpass filter on the LVCMOS output of the CDCE72010 eliminates the higher-order harmonics of the clock signal that help create fast rising and falling edges. The scope plot in Figure 13 demonstrates how the bandpass filter drastically reduces the slew rate of the unfiltered LVCMOS output and turns the square wave into a sine wave.

Figure 13. Impact of clock filter on sampling clock's slew rate



$$t_{Aperture\_ADC} = \sqrt{\left[\frac{\sqrt{\left(10^{-\frac{SNR_{Measured}}{20}}\right)^2 - \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2}}{2\pi \times f_{IN}}\right]^2 - (t_{Jitter,Clock\_Input})^2} \qquad (4)$$

Table 3. Measured SNR and calculated jitter

DEVICE	THERMAL NOISE (MEASURED SNR AT f_{IN} = 10 MHz) (dBFS)	MEASURED SNR AT HIGH f_{IN} (JITTER-LIMITED) (dBFS)	CALCULATED APERTURE JITTER (fs)
ADS54RF63	64.4	61.0 (f_{IN} = 1 GHz)	~115
ADS5483	79.1	78.2 (f_{IN} = 100 MHz)	~85

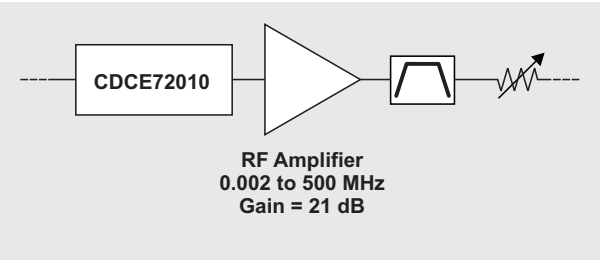
Table 4. SNR results with 90-fs clock jitter

DEVICE	CALCULATED SNR WITH 90-fs CLOCK JITTER (dBFS)	MEASURED SNR (dBFS)	CALCULATED JITTER FROM MEASURED SNR (fs)
ADS54RF63 (f_{IN} = 1 GHz)	59.9	58.7	~130
ADS5483 (f_{IN} = 100 MHz)	77.8	77.1	~125

One way to improve the slew rate is to add a low-noise RF amplifier with a fair amount of gain between the LVCMOS output of the CDCE72010 and the bandpass filter (see Figure 14). The amplifier should be placed before the filter so that its noise contribution to the clock signal is limited to the filter bandwidth and not to the clock input bandwidth of the ADC. Since the amplifier in the next experiment has a gain of 21 dB, a variable attenuator was added after the bandpass filter to match the slew rate of the filtered LVCMOS signal to the filtered output of the clock generator. The attenuator also protects the clock input of the ADCs from exceeding the maximum ratings.

With the low-noise RF amplifier included in the clock's input path, the SNR measurement at high input frequency was repeated for both data converters. The results are shown in Table 5. It can be observed that the measured SNR matches the predicted SNR very well. Using Equation 5 below provided calculated clock-jitter values that are within 5 fs of the 90-fs clock jitter, which was derived from the phase-noise measurement.

Figure 14. RF amplifier added in front of bandpass filter to reduce slew rate



Experiment with unfiltered sampling clock

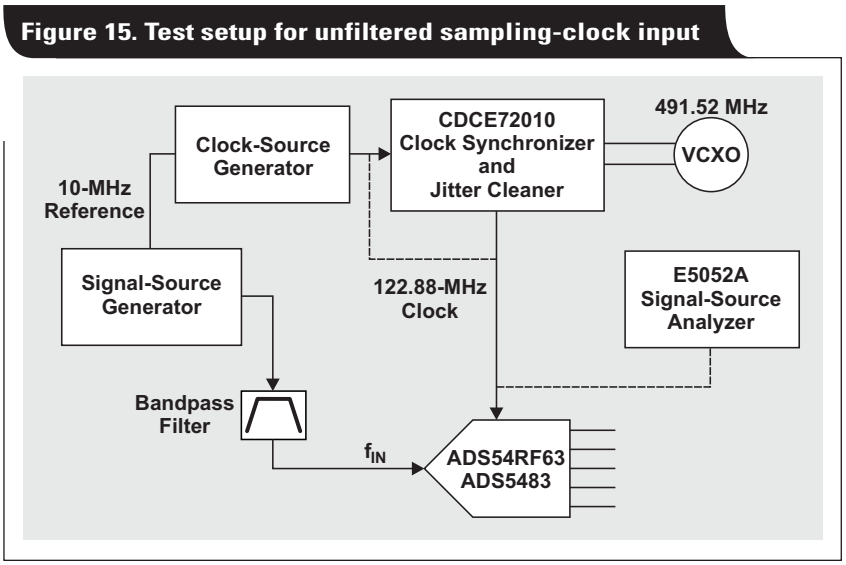
To stress the importance of filtering the sampling clock, the clock bandpass filter was removed from the CDCE72010 output in the next experiment. The E5052A phase-noise analyzer was used to capture the clock phase noise as shown in the setup in Figure 15. Unfortunately, however,

Table 5. SNR results with 90-fs clock jitter and RF amplifier

DEVICE	CALCULATED SNR WITH 90-fs CLOCK JITTER (dBFS)	MEASURED SNR WITH RF AMPLIFIER (dBFS)	CALCULATED JITTER FROM MEASURED SNR (fs)
ADS54RF63 (f_{IN} = 1 GHz)	59.9	60.0	~85
ADS5483 (f_{IN} = 100 MHz)	77.8	77.6	~95

$$t_{Jitter,Clock\_Input} = \sqrt{\left[\frac{\sqrt{\left(10^{-\frac{SNR_{Measured}}{20}}\right)^2 - \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2}}{2\pi \times f_{IN}}\right]^2 - (t_{Aperture\_ADC})^2} \quad (5)$$

Figure 15. Test setup for unfiltered sampling-clock input



the analyzer measures the phase noise only up to a 40-MHz offset of the carrier frequency and doesn't give any clue about the phase-noise characteristic beyond that point.

To set the correct upper integration limit when an unfiltered clock is used, the sampling theory has to be reviewed again. The unfiltered clock output of the CDCE72010 looks like a square wave with fast rising and falling edges caused by the higher-order harmonics of the fundamental sinusoid of the clock frequency. These harmonics have lower amplitude than the fundamental, and their amplitude decreases as the harmonic order increases.

At the sampling instant, both the fundamental sine wave and the higher-order harmonics mix with the input signal as illustrated in Figure 16. (For simplification, only one harmonic is shown.) Therefore, the phase noise around the third-order harmonic (for example) mixes with the input signal, and the third harmonic creates a mixing product as well. However, since the third harmonic of the clock signal has lower amplitude, the amplitude of this mixing product is also reduced.

When the two sampled signals are combined, it can be seen that the overall degradation of the phase noise caused by the third harmonic becomes minimal once the amplitude difference exceeds ~3 dB. Since the crossover point between the fundamental and the third harmonic is at $2 \times f_s$, integrating the wideband phase noise to $2 \times f_s$ should give a fairly accurate result.

As shown later in Figure 19, the phase noise of the unfiltered LVCMOS output of the CDCE72010 levels out around –153 dBc/Hz, starting at an offset frequency of

Figure 16. Clock fundamental and its harmonics mix with input signal at sampling instant

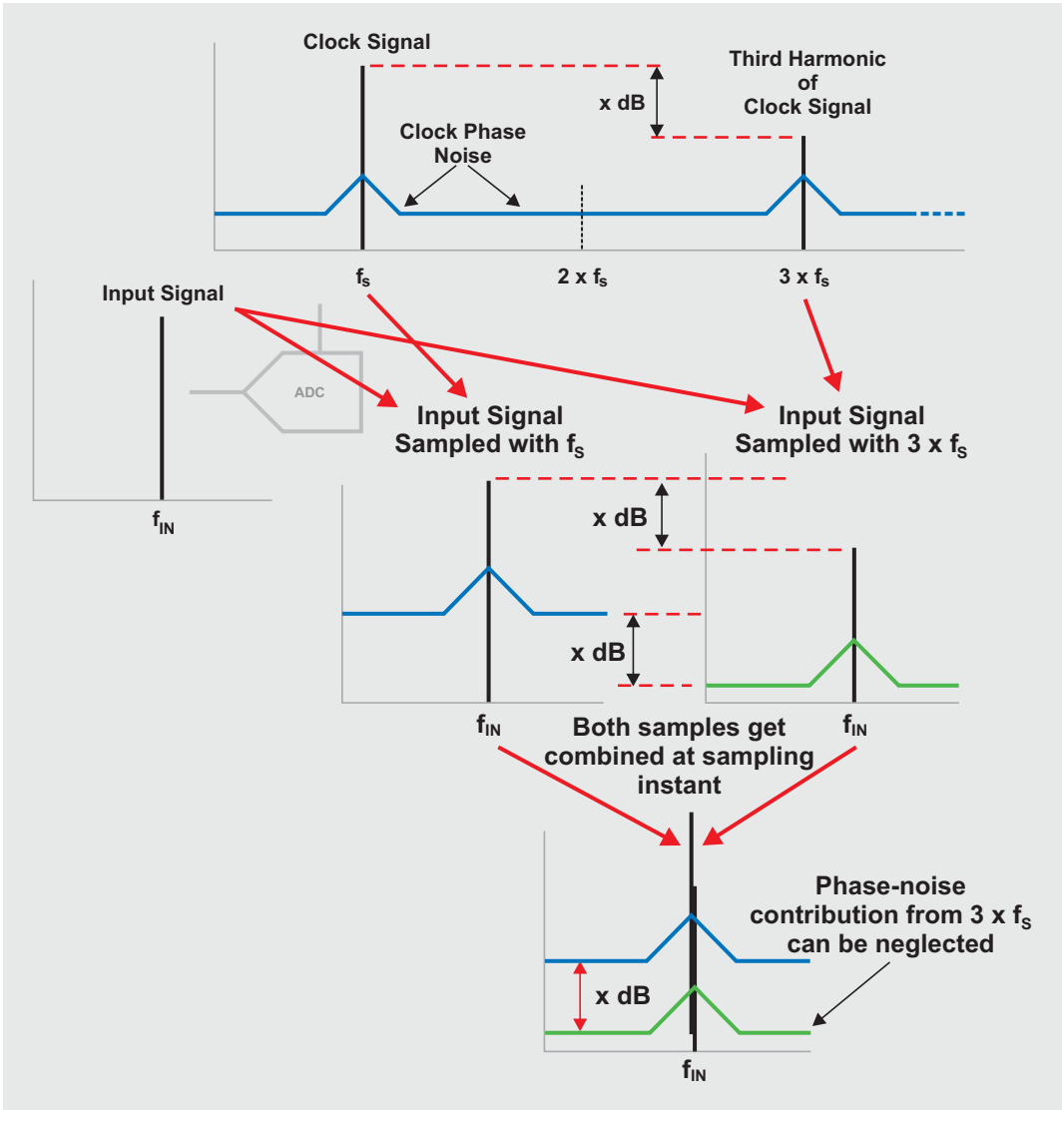


Table 6. SNR results with 1.27-ps clock jitter

DEVICE	CALCULATED SNR WITH 1.27-ps CLOCK JITTER (dBFS)	MEASURED SNR (dBFS)	CALCULATED JITTER FROM MEASURED SNR (fs)
ADS54RF63 (f_{IN} = 1 GHz)	42.8	51.35	~450

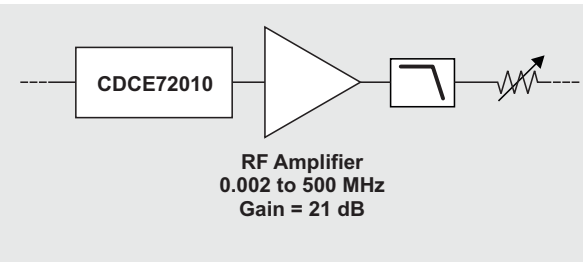
~10 MHz, which is likely due to the thermal noise of the LVCMOS output buffer. The ADS54RF63 EVM has a clock input bandwidth of ~1 GHz (limited by the transformer); hence, theoretically the phase noise should be integrated to ~1 GHz (rolling off at 3 dB at a 900-MHz offset). This would result in ~1.27 ps of sampling-clock jitter and would reduce the SNR at f_{IN} = 1 GHz to ~42.8 dBFS!

The actual SNR measurement was quite a bit better than that, as demonstrated in Table 6. There is a huge gap between the calculated clock jitter and the SNR compared to the actual measurement. This suggests that the phase noise of the LVCMOS output indeed is limited well before the 900-MHz offset boundary set by the transformer.

To prove that the phase noise of the unfiltered clock signal needs to be integrated to roughly twice the sampling frequency, the following experiment was set up: Different low-pass filters were added between the CDCE72010 output and the clock input of the ADS54RF63.

It is important to remember that a low-pass filter with a bandwidth of less than 3x the clock frequency reduces the slew rate of the clock signal just like the bandpass filter did in the earlier experiment. The low-pass filter eliminates the higher-order harmonics that produce the faster rise time and slew rate of the clock signal, thus increasing the aperture jitter of the ADC. For that reason, the same low-noise RF amplifier from the earlier experiment was added to the clock path, and the slew rate was matched to the signal generator by using the variable attenuator (see Figure 17).

Figure 17. RF amplifier added in front of low-pass filter to reduce slew rate



Using low-pass filters with different corner frequencies on the sampling clock of the ADS54RF63 (as depicted in Figure 18) resulted in the interesting values in Table 7. The results of this experiment suggest that the phase-noise impact of the LVCMOS output on the clock jitter is limited to roughly 200 to 250 MHz, which corresponds to an 80- to 130-MHz offset from the 122.88-MHz clock signal and is approximately 2x the sampling frequency. Therefore,

Table 7. Measured SNR for ADS54RF63

FILTER TYPE	MEASURED SNR AT f_{IN} = 1 GHz (dBFS)
Unfiltered Clock	51.35
140-MHz Low-Pass Filter	54.01
200-MHz Low-Pass Filter	51.81

Figure 18. Different low-pass filters limit phase noise

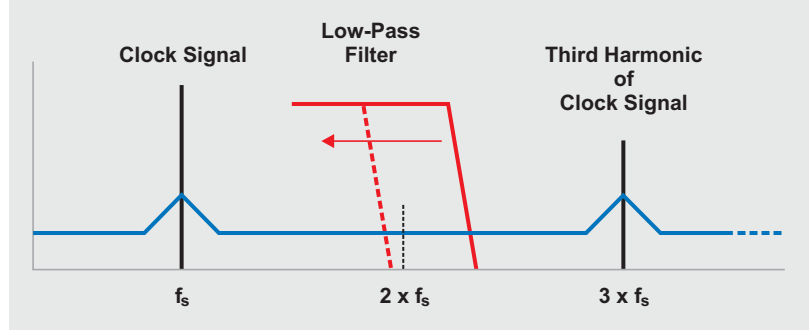


Table 8. SNR results with 445-fs clock jitter

DEVICE	CALCULATED SNR WITH 445-fs CLOCK JITTER (dBFS)	MEASURED SNR (dBFS)	CALCULATED JITTER FROM MEASURED SNR (fs)
ADS54RF63 (f_{IN} = 1 GHz)	51.6	51.35	~460
ADS5483 (f_{IN} = 100 MHz)	71.2	70.60	~480

Table 9. Measured SNR with filtered and unfiltered clock

DEVICE	BANDPASS-FILTERED CLOCK (dBFS)	UNFILTERED CLOCK (dBFS)	BANDPASS-FILTERED CLOCK WITH EXTERNAL AMPLIFIER (dBFS)
ADS54RF63 (f_{IN} = 1 GHz)	58.7	51.35	60.0
ADS5483 (f_{IN} = 100 MHz)	77.1	70.60	77.6

extending the wideband phase noise out to a 123-MHz offset results in a clock jitter of ~445 fs, as can be seen in Figure 19. Ideally the lower integration limit should be at 500 Hz (because of the chosen 131,000-point FFT); however, the jitter contribution from a 500-Hz to 1-kHz offset is extremely low, so it was neglected here in this measurement for simplification.

With the adjusted phase-noise plot, the calculated jitter matches the SNR measurement results very well, to within 10 to 30 fs for both the ADS54RF63 and the ADS5483 (see Table 8). Considering that there is probably a minor clock-jitter contribution from the phase noise around the third harmonic, the calculated SNR is a very close estimation.

Conclusion

This article has shown how to properly estimate a data converter's SNR when a filtered or unfiltered clock source is used. The results are summarized in Table 9. While a bandpass filter on the clock input is necessary to minimize the clock jitter, experiments showed that it reduces the clock slew rate and degrades the aperture jitter of the ADC. Therefore, the optimum clocking solution consists of a bandpass filter to limit the phase-noise contribution as well as some amplification of the clock amplitude and slew rate to minimize the aperture jitter of the ADC.

Part 3 of this article series will show some practical implementations on how to boost the performance of existing clocking solutions.

Reference

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1. Thomas Neu, "Clock jitter analyzed in the time domain, Part 1," *Analog Applications Journal* (3Q 2010) slyt379

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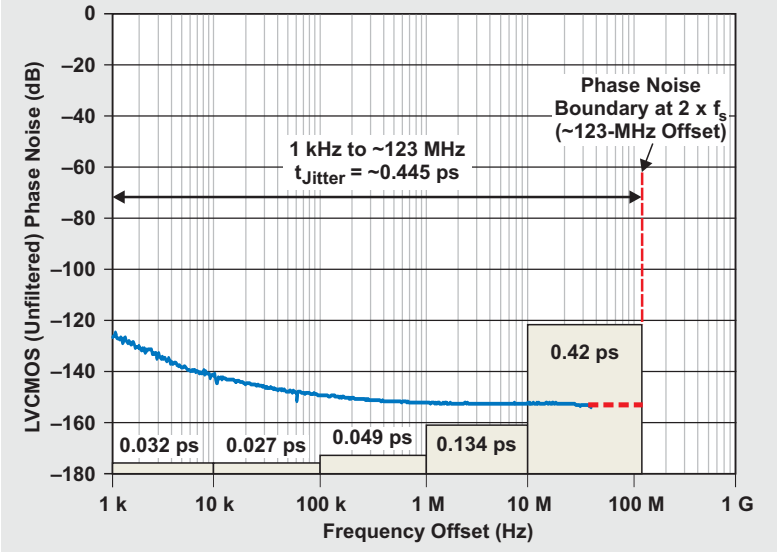
Replace *partnumber* with ADS5483, ADS54RF63, or CDCE72010

Figure 19. Unfiltered phase noise extrapolated to 123-MHz offset



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