Designing a negative boost converter from a standard positive buck converter

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Introduction

There are very few options for the designer when it comes to creating negative voltage rails in point-of-load applications. Integrated devices that are specifically designed for this are uncommon, and other available options typically have significant drawbacks, such as being too large, noisy, inefficient, etc. If a negative voltage is available, it is advantageous to use that as the input for the converter. This article describes a method using a standard positive buck converter to form a negative boost converter, which takes an existing negative voltage and creates an output voltage with a larger (more negative) amplitude. Using a boost regulator results in a smaller, more efficient, and more cost-effective design. A complete design example using an integrated FET buck converter is provided here. The basic theory of operation, high-level design trade-offs, and closed-loop compensation design of the resulting converter are discussed.

Negative boost topology

Implementing a negative boost converter takes advantage of some parallels between the power design and control of a positive buck converter and a negative boost converter. Figure 1 depicts the basic operation of a positive buck regulator. The buck consists of a half bridge that chops V_{IN} and a filter to extract the DC component. The filtered output voltage is regulated by varying the duty cycle (D) of the upper FET. When V_{OUT} is too low, the control loop reacts by causing D to increase. When V_{OUT} is too high, D is decreased. The buck input current is discontinuous (has a higher RMS current), and the output current is continuous and equal to the inductor current waveform. The current flow through the inductor is positive, flowing away from the half bridge.

Figure 2 depicts the negative boost topology in which a more negative voltage is generated from an existing negative voltage. During D, the inductor current is increased, storing energy ($dI = –V_{IN} \times D \times T/L$). During 1 – D, the energy is transferred to the output. When the upper FET is turned off and the lower FET is turned on, the inductor current flows into the output, supporting the load as the inductor current decreases. From Figures 1 and 2 it can be seen that the negative boost regulator resembles the positive buck regulator, except that it is level shifted below ground. Also, V_{IN} and V_{OUT} are transposed. Notice these common features:

- The upper FET is the controlled switch.
- The inductor current flows in the same direction through the inductor (away from the half bridge).
- Increasing V_{OUT} results from increasing D.

Figure 1. Simplified positive synchronous buck regulator

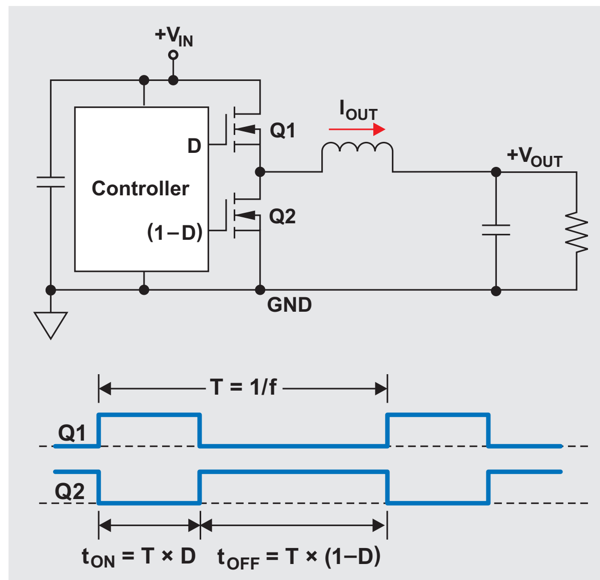


Figure 2. Simplified negative synchronous boost regulator

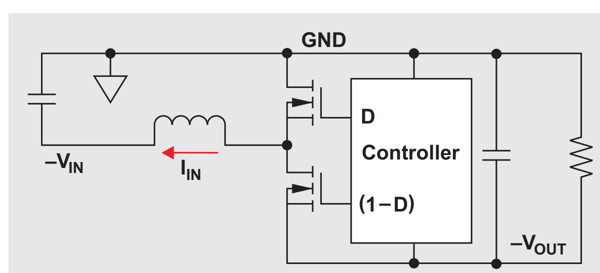
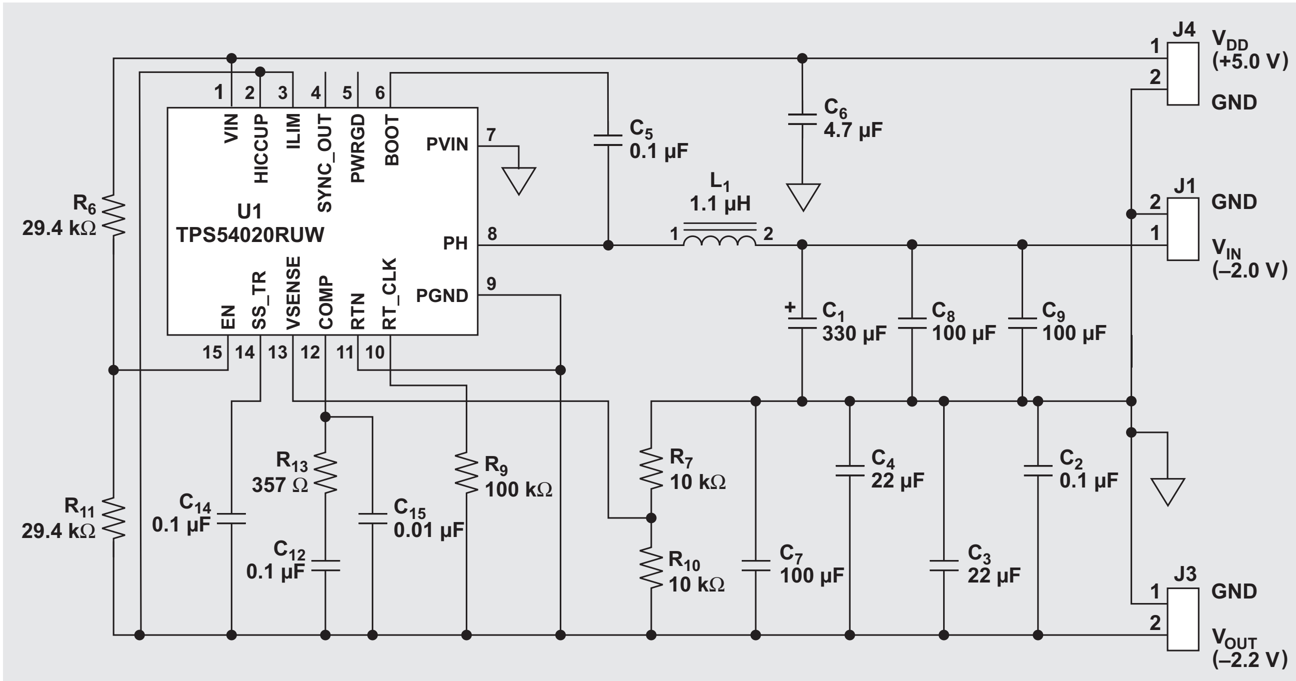


Figure 3. Complete schematic of the example negative boost regulator



The significance of these similarities is that the negative boost converter can be constructed by using a readily available positive buck converter. One difference in operation is that the boost converter has a discontinuous output current and a continuous input current, the opposite of the buck converter.

Converter selection

There are three additional things that need to be considered when selecting a converter:

1. The converter should have external compensation to accommodate the different control algorithm associated with the boost converter, which will be discussed later.
2. The converter is processing current equal to the input current, not the load current, so the current rating and current limit need to be sized accordingly. For instance, neglecting the effects of efficiency (η), a 12-W, –6-V to –12-V boost converter has an output current of 1 A (12 W) and an input current of 2 A (12 W). A converter with a current rating greater than 2 A is required for this design. The output-current rating of the converter selected must be greater than that in Equation 1:

$$I_{RATING} = \frac{P_{OUT}}{\eta V_{IN(min)}}. \qquad (1)$$

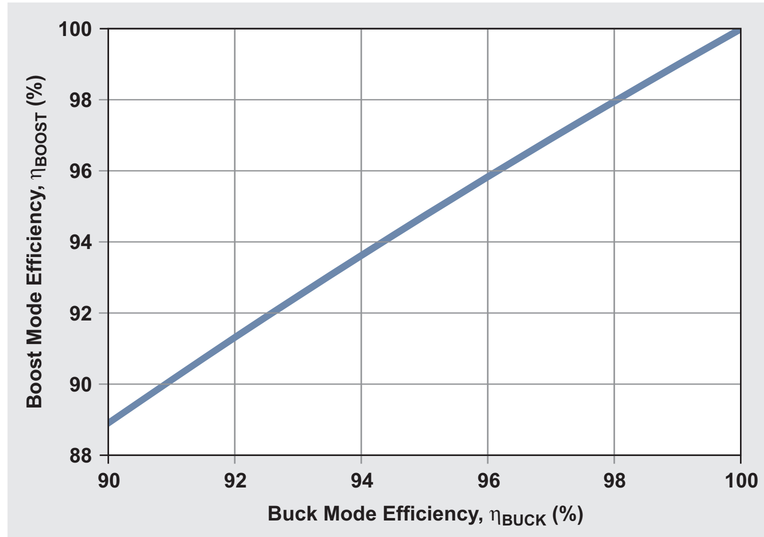
3. The converter's V_{DD} is biased by $-V_{OUT}$. When the converter is first powered on, V_{OUT} equals V_{IN}, and V_{OUT} is increased until it is in regulation. Therefore, the controller specification should allow the converter to start with $V_{DD} = |-V_{IN}|$, and the converter should be rated to operate with $V_{DD} = |-V_{OUT}|$. For instance, a design that converts a –6-V input to a –12-V output requires the controller to start with V_{DD} = 6 V and to continue running after start-up with V_{DD} = 12 V. This can be a problem when the negative input is a low voltage. A solution is to use a converter that has a V_{DD} separate from the power supply's V_{IN}. Figure 3 shows a negative boost regulator designed to convert –2.0 V to –2.2 V by using the TPS54020 from Texas Instruments (TI). Although this is a relatively low-voltage regulator, the principle is the same for any $-V_{IN}$ and $-V_{OUT}$ as long as the converter specifications support the voltages. Notice that the power to U1, pin VIN, is separate from the power ground to pin PVIN, allowing low-voltage operation.

As previously mentioned and defined in Equation 1, the current rating of the converter is driven by input current. Therefore, the power dissipation in the converter is dependent on input current.

The efficiency of the negative boost regulator (η_{BOOST}) is related to that of the positive buck regulator (η_{BUCK}) but is slightly lower. Figure 4 and Equation 2 show the relationship of the two efficiencies, which are about equal when the specified η_{BUCK} is above 90%:

$$\eta_{BOOST} = \frac{2\eta_{BUCK} - 1}{\eta_{BUCK}} \quad (2)$$

Figure 4. Efficiency of negative boost regulator



Component selection

The inductor can be chosen by using the same criteria as defined in the buck converter's datasheet. The boost converter's input and output capacitors should be chosen based on ripple voltages required by the application, keeping in mind that the output capacitor must be rated for the higher RMS current.

Control theory

Boost converters have a different, more complicated transfer function than buck converters. As with buck converters, the transfer function is different between voltage-mode control and current-mode control. This analysis uses a current-mode-controlled boost converter based on the TPS54020, a current-mode device. The Bode-plot method is used to evaluate the stability of this control-loop design. Points of interest for stability are the phase when the open-loop gain crosses unity, and the gain when the phase crosses –180°. The open-loop gain is equal to the forward transfer function multiplied by the control transfer function, including all gains around the control loop.

The current-mode power stage ("plant" in control jargon) has the forward transfer function given in Equation 3:[1]

$$G_{PS}(s) = \frac{g_M \times R_{LOAD} \times (1 - D)}{2} \times \frac{\left(1 + \frac{s}{2\pi \times f_{ESR}}\right)\left(1 - \frac{s}{2\pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2\pi \times f_P}} \times H_e(s), \quad (3)$$

where s is the complex Laplace variable and $H_e(s)$ represents the higher-frequency dynamics. The continuous boost has two salient control features. First, the plant is a single-pole system, owing to the effect of current-mode control. Second, there is a right-half-plane zero (RHPZ).[1, 2] The RHPZ, plant pole, and C_{OUT} equivalent-series-resistance (ESR) zero frequencies are described respectively by the following equations:

$$f_P = \frac{2}{2\pi R_{LOAD} C_{OUT}} \quad (4a)$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (4b)$$

$$f_{RHPZ} = \frac{R_{LOAD}}{2\pi L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \quad (4c)$$

The RHPZ requires that the unity-gain bandwidth of the loop be less than the minimum RHPZ frequency, usually by a factor of 5 to 10. If lower bandwidth is desired, the RHPZ can be ignored, and so can $H_e(s)$ in Equation 3. This design uses ceramic output capacitors, so the ESR zero also can be ignored. Now the control equations simplify to

$$G_{PS}(s) = \frac{g_M \times R_{LOAD} \times (1 - D)}{2 \times \left(1 + \frac{s}{2\pi \times f_P}\right)}. \quad (5)$$

Equations 3 and 5 are modified, using g_M (the compensation to output-current gain in A/V) instead of R_{SENSE}, with $g_M = 1/R_{SENSE}$.

Designing a negative boost regulator

It has been established that the forward transfer function simplifies to a single-pole system as described by Equation 5. A real control-loop example can be based on a design using TI's TPS54020EVM082, with $V_{IN} = –2.0$ V, $V_{OUT} = –3.0$ V, and $I_{OUT} = 6$ A. This electrical design can be reconfigured as a negative boost regulator consistent with the circuit in Figure 3, using many of the same components as in the EVM design. The terms "input" and "output" from here on refer to the boost mode input and output. Equation 4 can be used to calculate the minimum RHPZ as 32 kHz. The goal of the control-loop design is to have a unity-gain crossover at 1.0 kHz, so the effects of both the ESR zero and the RHPZ can be ignored.

Table 1 contains some specific parameters and values. Equation 6 uses these values to describe the forward transfer function:

$$G_{PS}(s) = \frac{R_{LOAD} \times 5.70}{1 + \frac{s \times R_{LOAD}}{13889}} \quad (6)$$

The Bode plot of $G_{PS}(s)$ is depicted in Figure 5 for four different load-resistance values. Note that the pole location and low-frequency gain are functions of load resistance. Also note that the gain slope does not vary after the pole (driven by C_{OUT}). Before the pole, the gain is dependent on the load, with the highest-frequency pole at the maximum load (minimum R_{LOAD}). A 0.5-Ω load (I_{LOAD} = 6.0 A) results in a pole at 4.4 kHz. It can also be seen that the RHPZ causes the gain to rise and the phase to fall, which makes compensation impossible and requires crossover to occur before the effect of the RHPZ becomes detrimental.

The plan for this design is to have unity gain in the open-loop transfer function at 1.0 kHz. The plant has a gain of approximately +9 dB at 1.0 kHz. This forward transfer function can be compensated easily with an integrator followed by a zero at the highest $G_{PS}(s)$ pole frequency, and with an overall gain that results in about –9 dB at the desired crossover of 1.0 kHz (+9 dB + –9 dB = 0 dB). This compensation approximates a single-pole rolloff characteristic through crossover and results in sufficient phase margin.

Bode stability criteria

A closed-loop system with negative feedback has a transfer function as in Equation 7:

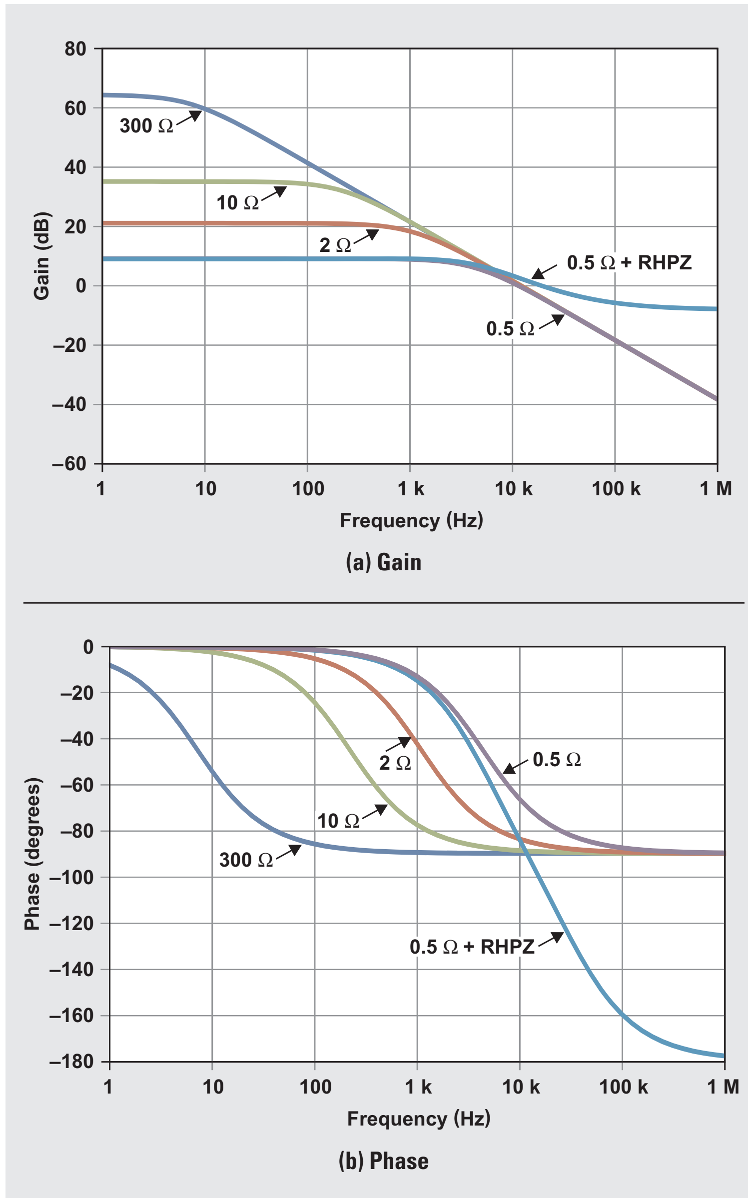
$$Y(s) = \frac{G(s)}{1 + G(s)H(s)}, \quad (7)$$

where G(s) is the forward (plant) transfer function, H(s) is the negative feedback control, and G(s)H(s) is the open-loop transfer function. The Bode stability criteria state that Y(s) is rational except where G(s)H(s) = –1. In the latter case, Y(s) is infinite and unstable. Two things have to happen at the same time for instability to occur. First, |G(s)H(s)| must equal 1 (gain = 0 dB); second, the phase of G(s)H(s) must equal –180°, corresponding to –1. Bode plots, including both the phase margin and the gain margin, are used to evaluate how near to this condition a control design approaches. Phase margin is defined as the phase difference between G(s)H(s) and –180° when the gain equals 0 dB, and gain margin refers to the negative gain when the phase equals –180°. A phase margin greater than 45° is generally considered good in power-supply design.

Table 1. Design values and TPS54020 datasheet[3] parameters for negative boost regulator

PARAMETER	COMMENTS
C_{OUT} = 144 µF	
L = 1.1 µH	
g_M = 17 A/V = 1/R_{SENSE}	g_M from datasheet = I_{SWITCH}/V_{COMP}
g_{EA} = 0.0013 A/V	From datasheet
D = (V_{OUT} – V_{IN})/V_{OUT} = 0.33	
V_{REF} = 0.600 V	From datasheet
R_{10} = 10.0 kΩ; R_7 = 40.2 kΩ	Feedback-divider gain = 0.2 V/V

Figure 5. Bode plots of $G_{PS}(s)$ for four different load resistances



Error-amplifier compensation

The error amplifier (EA) is depicted in Figure 6, and the circuit's transfer function is described by

$$G_{EA}(s) = \frac{g_{EA}R_{10}}{R_{10}+R_7} \times \frac{1}{C_1+C_{15}} \times \frac{1}{s} \times \frac{C_{15}R_1 s + 1}{\frac{C_1C_{15}}{C_1+C_{15}} \times R_1 s + 1}. \quad (8)$$

Note that the transfer function of the transconductance error amplifier includes the feedback-divider gain. If this was a voltage-feedback error amplifier, the divider would not be a gain term. Inspection of Equation 8 finds that $G_{EA}(s)$ has a pole at 0 Hz, a compensating zero at

$$f = \frac{1}{2\pi R_1 C_{15}},$$

and a higher-frequency pole at

$$f = \frac{1}{2\pi R_1\left(\frac{C_1C_{15}}{C_1+C_{15}}\right)}.$$

Note that if the zero and pole are separated by a decade or more, then $C_{15} >> C_1$. The plan is to set the gain equal to –9 dB at 1.0 kHz, place the zero at the highest $G_{PS}(s)$ pole (4.4 kHz) to compensate the pole in the plant, and place the additional pole at some higher frequency.

Evaluating $|G_{EA}(s)|$ at f = 1.0 kHz and setting it equal to –9 dB yields $C_1 + C_{15} \approx C_{15} = 0.117$ µF. The nearest standard value of 0.10 µF is chosen. Given C_{15} and the desired zero location of 4.4 kHz, R_1 can be calculated as 360 Ω. The nearest standard value of 357 Ω is chosen. The higher-frequency pole is placed at 50 kHz. This is rather arbitrary, but this pole needs to be greater than 10 times the crossover frequency to ensure that it doesn't degrade the loop-phase margin. Adding this high-frequency pole is desirable because it keeps the loop gain decreasing at higher frequency. C_1 is calculated to be 0.01 µF. Figure 7 shows the Bode plot of the converter's final compensated loop. The predicted and measured open-loop gain and phase match closely near the 1.0-kHz unity-gain crossover.

Test data

Figure 7 also includes the measured Bode plot of the power supply with a 0.5-Ω load. There is good correlation near the 1.0-kHz crossover. The predicted waveforms in Figure 7 also include the effects of the RHPZ. The gain and phase disturbance between 1.0 kHz and 10 kHz is thought to result from a nonlinear characteristic in the controller and only begins to appear at load currents above 50%. Since this occurs above the crossover, it is inconsequential to the stability of the loop.

Figure 6. Error amplifier and compensation

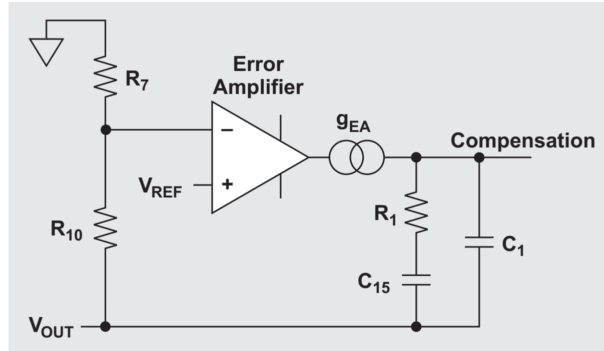
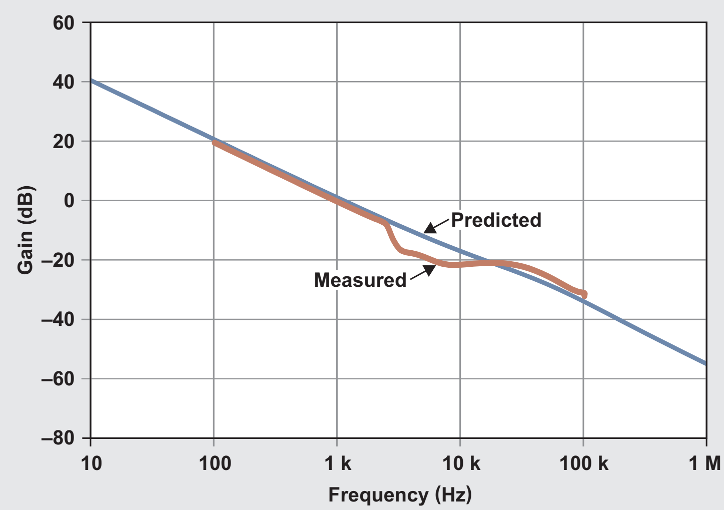
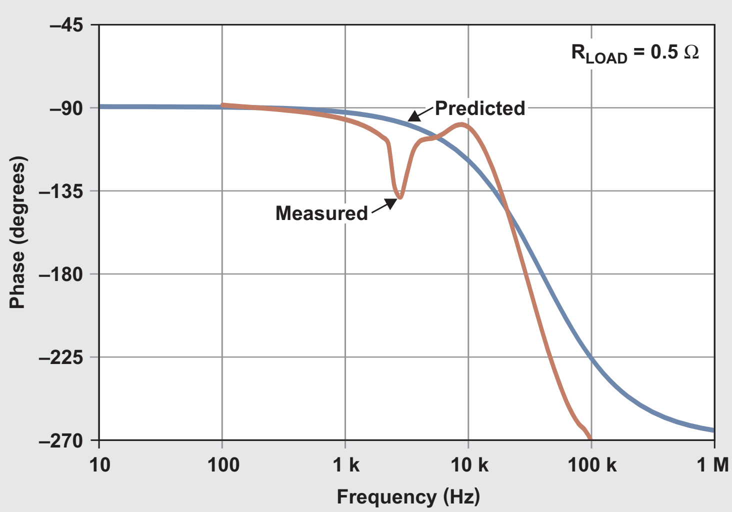


Figure 7. Bode plot of converter's final compensation loop



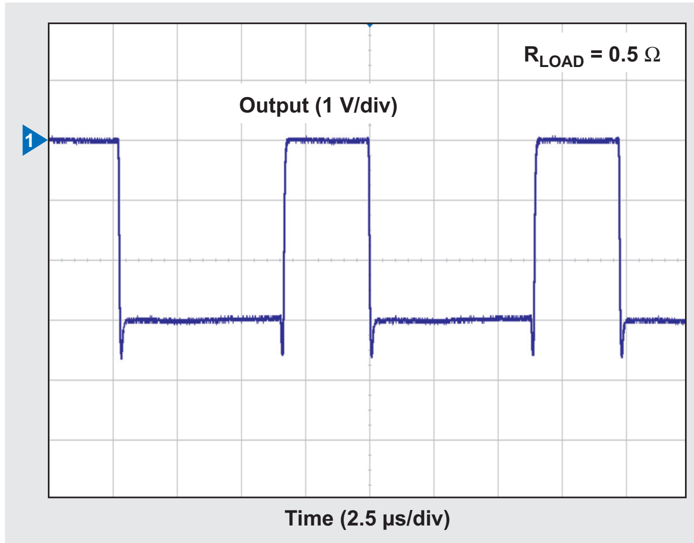
(a) Open-loop gain



(b) Open-loop phase

Figure 8 shows the switching waveform with a load of 0.5 Ω (6 A). As expected, it looks identical to a buck converter's switching waveform but is level shifted below ground, riding on the programmed V_{OUT} of –3.0 V.

Figure 8. Switching voltage waveform



Additional considerations

Three additional points about this type of converter should be noted. First, the TPS54020 has a separate V_{IN} and V_{DD}. This enables power conversion from a low voltage (2 V in this case), which would not be possible with many other converters. Second, this negative-boost design concept is extendable to higher voltages and is limited only by the ratings of the converter selected. Third and most important, before the boost converter starts but after voltage is applied to the PVIN pin, any load current on the boost output is conducted through the body diode of the lower FET. Although the TPS54020 functions well, starting up even with a DC current, not all devices may perform in the same way. Therefore, it might be necessary to add a Schottky diode in parallel with the lower internal FET to provide an external path for this current.

Conclusion

This article demonstrates that a positive buck regulator can be used to implement a negative boost regulator and obtain good performance. The actual performance very closely matches the expected behavior, both in real-time measurements and in the Bode plot of the control loop.

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