Design Guide: TIDA-050022

Power Stage Reference Design for <100-VIN DC/DC Converters

Description

This reference design implements a high-frequency power stage design based on the UCC27282 120-V half-bridge MOSFET driver and CSD19531 100-V power MOSFETs. With efficient switches and flexible V_{GS} operating range, this design can reduce overall gate drive and conduction losses to achieve optimum efficiency. This power stage design can be widely applied to many space-constrained applications such as telecom brick-power modules, solar inverters, and DC motor drives.

Resources

TIDA-050022	Design Folder
UCC27282	Product Folder
CSD19531	Product Folder

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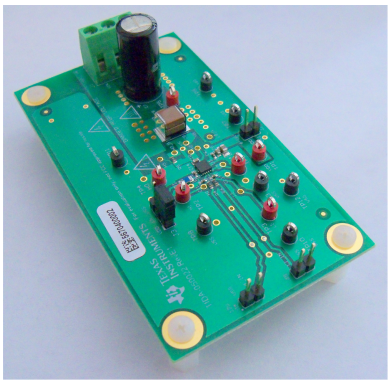
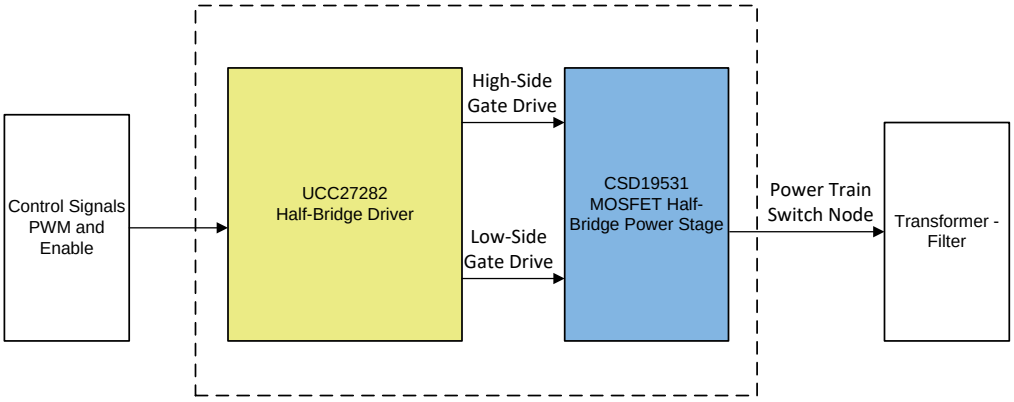
Applications

- Telecom brick-power module
- Solar micro inverter and power optimizer
- Server and network power supplies
- DC motor drives

Features

- Compact 100-V power-stage design with switching up to 1 MHz
- Independent Pulse Width Modulation (PWM) inputs for high side and low side with cross-conduction protection
- Low propagation delay of 16 ns, delay matching of 1 ns typical, 7 ns maximum
- Driver VDD operating range 6 V to 16 V
- Negative voltage capability tolerates high noise environments
- Enable with low standby current





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1 System Description

Telecom and datacom equipment capabilities keep increasing with demand for more processing power within a given size, or even size reduction as well. Increased capabilities of the equipment result in more demand from the power supplies. The power supplies in these systems must be optimized from a space utilization an efficiency standpoint. The complexity of control and interface is also increasing in telecom, datacom, and solar systems which make them more susceptible to noise and transients .

The half-bridge driver and power MOSFET power stage is used in a variety of DC/DC converter topologies including half-bridge, full bridge, synchronous buck, and full-bridge synchronous rectification. Solar micro inverters, solar optimizers and motor drive also use this power stage in many applications.

This reference design uses CSD19531 NexFET™ Si power MOSFETs and the UCC27282 120-V half-bridge driver to realize a power stage with high efficiency. The half-bridge driver allows two independent inputs for high-side and low-side gate drive and has cross conduction protection which turns off both gate drive signals in the event both inputs are high. The cross conduction protection does not have a fixed dead time so the controller can control precise timing of the turn on and turn off of the power MOSFETs.

This design can be applied to many high-efficiency applications such as telecom power modules, solar power, 48V server power, and industrial power supplies.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHARACTERISTICS					
Input and output voltage		0		100[(1)]	V
Input and output current		0	4	8	A
Bias voltage		6	8	16	V
LI and HI Inputs to VGS Delay			15	30	ns
Delay Matching	LI/HI Complimentary		1	7	ns
SYSTEM CHARACTERISTICS					
Switching frequency		10	200	1000	kHz
Efficiency	V_{IN} = 48 V, V_{OUT} = 24 V, I_{OUT} = 4 A, f_{SW} = 200, 300 kHz	94	95	95.3	%

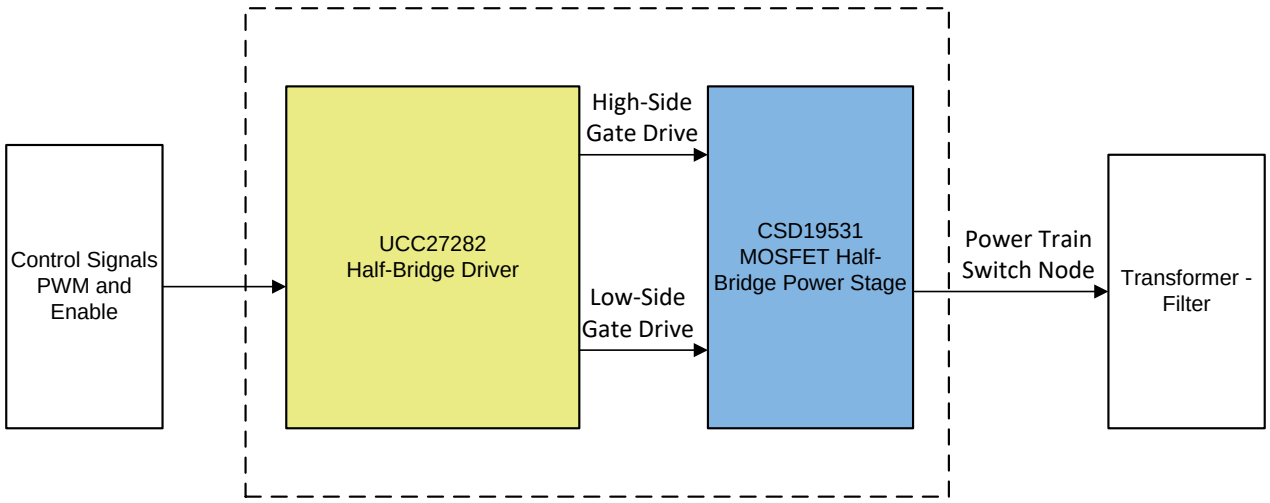
(1) HS voltage (MOSFET switch node) is limited to 100 V including overshoot. This may limit input voltage to a lower value.

2 System Overview

2.1 Block Diagram

Figure 1 shows the block diagram of this design. One half-bridge driver UCC27282 drives two MOSFETs in a half-bridge configuration. Two 100-V rated CSD19531 FETs are used as switching devices.

Figure 1. TIDA-050022 Block Diagram



2.2 Design Considerations

2.2.1 FET Selection

The majority of 48 V input voltage telecom and datacom power module designs have gate driver bias voltage (V_{DD}/V_{CC}) voltage in the 9 V to 10 V range using 100 V (V_{DS}) rated power MOSFETs. The gate drive losses are reduced with lower gate drive voltage (V_{GS}) and many MOSFET devices $R_{DS(on)}$ versus V_{GS} curves indicate that there is little reduction in $R_{DS(0n)}$ beyond 8 V to 10V V_{GS}. One consideration of selecting the driver V_{DD} is the turn on UVLO threshold and including some margin for negative voltage transients on the bias supply. This may result in selecting the driver V_{DD} to be higher than the optimum gate drive and conduction loss operating point when using previous generation drivers.

The CSD10531 100V 5.3 mΩ MOSFET total gate charge, or Q_G, vs V_{GS} and the $R_{DS(on)}$ vs V_{GS} can be viewed in the CSD19531 data sheet. Although this MOSFET has an $R_{DS(on)}$ specification with V_{GS} = 6 V you can see that the $R_{DS(on)}$ curve still has a noticeable declining $R_{DS(0n)}$ vs V_{GS} at 6 V. At V_{GS} = 8 V the curve slope is much lower.

The gate drive losses for each driver output channel are dependent on V_{DD}, switching frequency (F_{SW}), and MOSFET Q_G as shown in Equation 1.

$$P_{GD} = V_{DD} \times f_{SW} \times Q_G \quad (1)$$

Another consideration for applications which will have body diode conduction during the switching transitions such as synchronous buck or synchronous rectification is the body diode t_{rr} and Q_{rr}. The body diode reverse recovery losses delta can exceed conduction loss delta even though the $R_{DS(on)}$ is lower if the body diode reverse recovery time is longer. See Table 2 for parameter comparison of the CSD19531 MOSFET and CSD19533 MOSFET.

Table 2. Parameter Comparison of Switching FETs

PARAMETER	CSD19531	CSD19533
Max V_{DS} (V)	100	100
$R_{DS(on)}$ (mΩ), V_{GS}=10 V	5.3	7.8
$R_{DS(on)}$(mΩ), V_{GS}=6 V	6.0	8.7
Q_g (nC)	37	27
t_{rr} (ns), Body Diode	147	62
Q_{rr} (nC), Body Diode	226	163

2.2.2 Component Selection

2.2.2.1 Bootstrap and VDD Capacitor

The bootstrap capacitor must maintain the V_{HB-HS} voltage above the UVLO threshold for normal operation. To determine the minimum required bootstrap capacitance first calculate the maximum allowable drop across the bootstrap capacitor, ΔV_{HB}, with Equation 2.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} \tag{2}$$

where

- V_{DD} is the supply voltage of the gate driver device
- V_{DH} is the bootstrap diode forward drop
- V_{HBL} is the HB falling UVLO threshold ($V_{HBR(max)}$ - V_{HBH})

Many applications may target ripple voltage lower than the equation result, such as 0.5 V to 1 V ripple.

Determine the estimated charge per switching cycle from the bootstrap capacitor with Equation 3.

$$Q_{TOTAL} = Q_G + I_{HBS} \times \left(\frac{D_{MAX}}{f_{SW}} \right) \tag{3}$$

where

- Q_G is the total MOSFET gate charge
- I_{HBS} is the HB to VSS leakage current
- D_{Max} is the converter maximum duty cycle
- I_{HB} is the HB quiescent current

Once the total charge is known the minimum bootstrap capacitance can be determined as follows in Equation 4.

$$C_{BOOT(min)} = \frac{Q_{TOTAL}}{\Delta V_{HB}} \tag{4}$$

The bootstrap capacitor should be X7R or better dielectric with low inductance package(s). Also since the capacitance is reduced with DC bias, choose a capacitor with at least two times the expected maximum voltage in the application.

TI recommends the VDD capacitor value at least 10x the value of the bootstrap capacitance to minimize VDD ripple from charging the bootstrap capacitor. The VDD capacitor should also be X7R or better temperature stability dielectric. It is recommended to parallel a high frequency bypass capacitor in a small package size, 0402, and low value such as 1nF to filter high frequency noise with the VDD capacitor.

2.2.2.2 External Gate Resistor

In high frequency switching power supply applications where high-current gate drivers such as the UCC27282 are used, high current loops with parasitic inductances and parasitic capacitances can cause noise and ringing on the gate of power MOSFETs. Gate resistors are used often to damp this ringing and noise. There are also cases where gate resistance may be selected to address EMI and excessive switch node voltage spikes. It is good practice to make provisions for external gate resistors to allow addressing these possible issues.

Use the following equations to calculate the driver pullup and pulldown current.

The high-side driver pullup current can be determined with Equation 5.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{GATE} + R_{GFET(int)}} \quad (5)$$

where

- I_{OHH} is the high-side peak pullup current
- V_{DH} is the bootstrap diode forward drop
- R_{HOH} is the gate driver internal high-side pullup resistance. Value can be calculated from test conditions ($R_{HOH} = V_{HOH}/I_{HO}$)
- R_{GATE} is the external gate resistance between the driver output and MOSFET gate
- $R_{GFET(int)}$ is the MOSFET internal gate resistance in the MOSFET datasheet

The high-side driver sink current can be determined with Equation 6.

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{GATE} + R_{GFET(int)}} \quad (6)$$

where

- I_{OLH} is the high-side peak pullup current
- R_{HOL} is the gate driver internal high-side pull-down resistance. Value can be calculated from test conditions ($R_{HOL} = V_{HOL}/I_{HO}$)

The low-side driver pullup current can be calculated with Equation 7.

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{GATE} + R_{GFET(int)}} \quad (7)$$

where

- R_{LOH} is the gate driver low-side pullup resistance

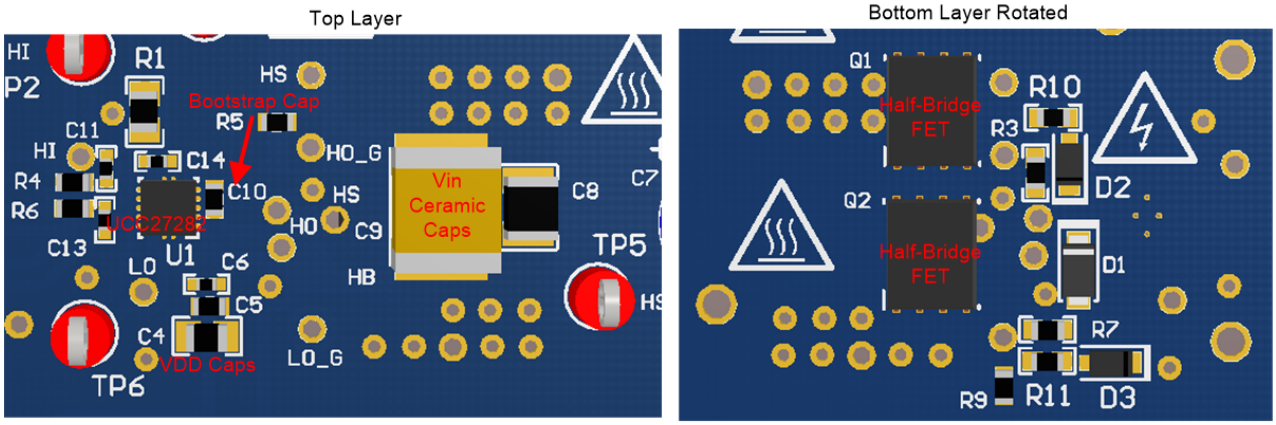
The low side driver sink current can be determined with Equation 8.

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{GATE} + R_{GFET(int)}} \quad (8)$$

2.2.3 Layout Considerations

To achieve best performance the layout of the 100-V power stage requires attention to the loop inductance for both the power loop and gate drive loop. Figure 2 shows a general view of the layout.

Figure 2. Layout General View



2.2.3.1 Gate Drive Loop Layout

Figure 3 and Figure 4 show the layout of the gate loop of the upper and lower FETs. To achieve the minimum loop inductance, the layout of gate drive loop must follow these rules:

- Have the VDD capacitor or bootstrap capacitor as close as possible to the gate driver because these traces will be part of the gate loop.
- Use a dedicated Kelvin source or minimum sharing of source trace between the gate drive loop and main power loop to achieve the minimum common source inductance. The high di/dt on the power loop can easily be coupled to the gate drive loop. This may cause decreased switching speed and other negative effects.
- To keep the return loops as short as possible, vias in pads are used in this design to further reduce the parasitic inductances and improve the current extraction from components.

Figure 3. Gate Drive Loop Layout for High-Side FET

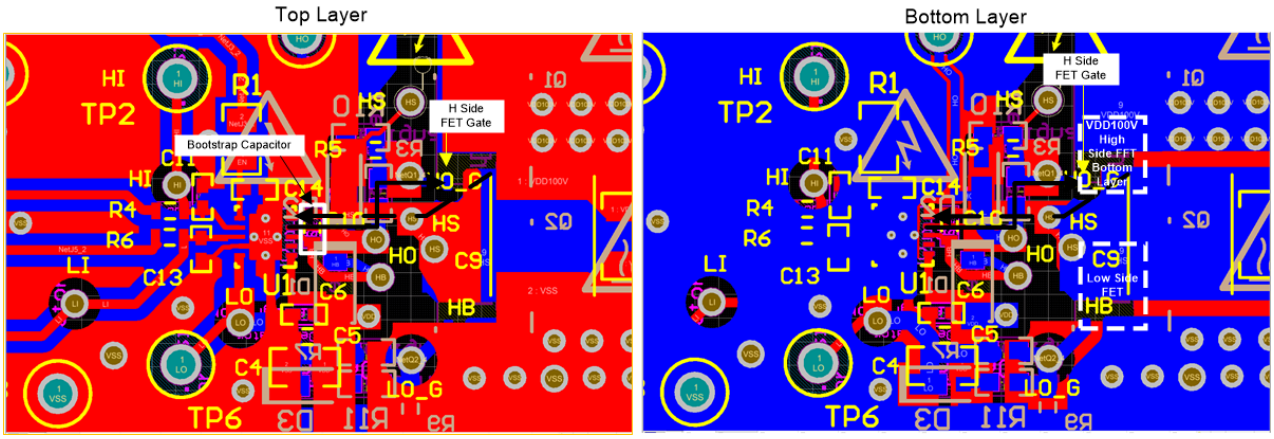
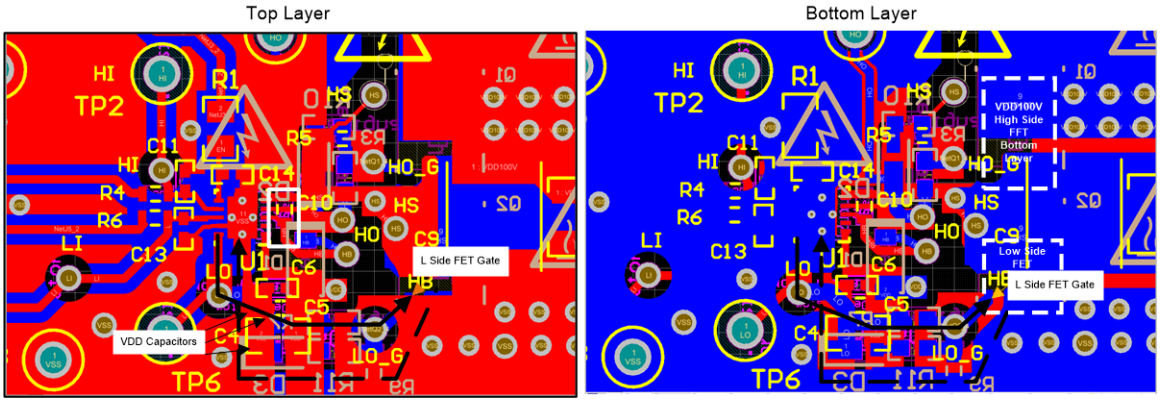


Figure 4. Gate Drive Loop Layout for Low-Side FET



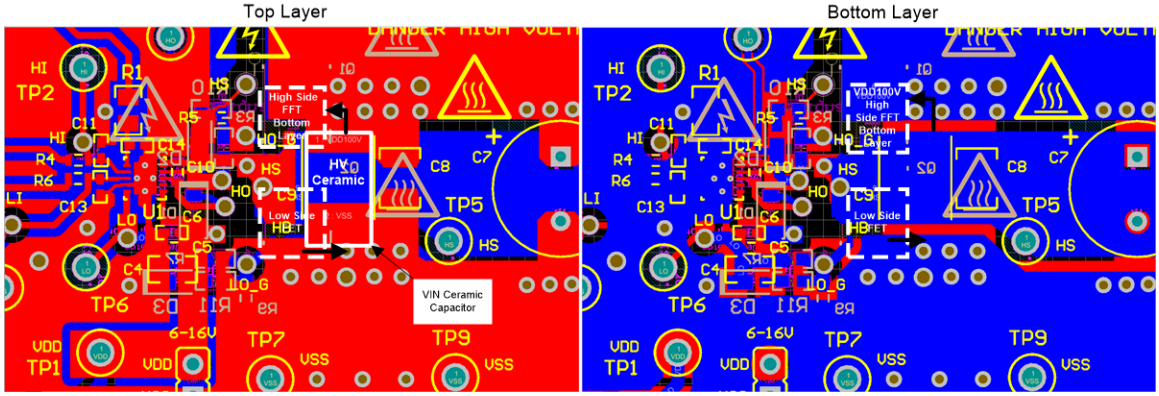
2.2.3.2 Power Loop Layout

The power loop layout objective is to minimize stray inductance. To realize a small power loop:

- Place ceramic capacitors with a small package as close to the devices as possible. These capacitors are usually better in frequency response and have a high bandwidth to absorb high-frequency noise generated during switching than bulk capacitors.
- A compact component placement is needed. Place the upper and lower FETs stacked from VIN to the power ground as close as possible to the input voltage (V_{IN}) capacitors.
- Minimize the overlap between switching node and ground/Vin copper. This overlap avoids the extra parasitic capacitance, which adds to C_{OSS} of FETs. If not designed well, the parasitic capacitors can generate significant loss at high switching frequency.

Figure 5 shows that the size of the power loop is minimized. The ceramic capacitors are placed across VIN and ground with multiple vias connecting the other layer planes close to the FETs.

Figure 5. Half-Bridge Power Loop Layout



2.3 Highlighted Products

2.3.1 UCC27282

The UCC27282 is a 120-V, half-bridge, high-performance MOSFET driver designed for applications that require high drive strength, wide bias voltage operating range, low propagation delays and excellent delay matching.

The UCC27282 half-bridge driver has new features and parameter improvements to achieve optimum power module performance and enhance robustness. The wide operating VDD range of 6 V to 16 V with adequate gate drive strength enhances flexibility to optimize efficiency based on gate drive losses, resistive losses and switching loss. A low signal on the EN pin disables the driver and sets the UCC27282 in a state of low bias current I_{DD} typically 7 µA. This low current will help achieve low standby power when the module is disabled. High-frequency operation and precise timing can be achieved due to low typical propagation delay of 16 ns and typical delay matching of 1 ns.

The UCC27282 includes an input interlock feature which prevents both gate driver outputs from being in the high state at the same time in the event both inputs are high. This will prevent cross conduction of the power MOSFETs in the case of unexpected disturbance or noise on the driver inputs. The UCC27282 operates over a wide temperature range from –40°C to +140°C and is offered in a small 3 x 3 QFN package.

2.3.2 CSD19531

The CSD19531 is a 100-V N-Channel NexFET™ designed to minimize loss in power conversion applications. The $R_{DS(on)}$ is rated at 6.0 mΩ and 5.3 mΩ at V_{GS} of 6V and 10 V. The Q_G is only 37 nC at 10 V V_{GS} resulting in low gate drive loss.

The CSD19531 5-mm x 6-mm SON package has very low thermal resistance and is a common package size. The CSD19531 is also avalanche rated to improve the robustness of the power converter design.

The CSD19531 is well suited for power conversion applications including primary side telecom, secondary side synchronous rectification, and motor drive.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

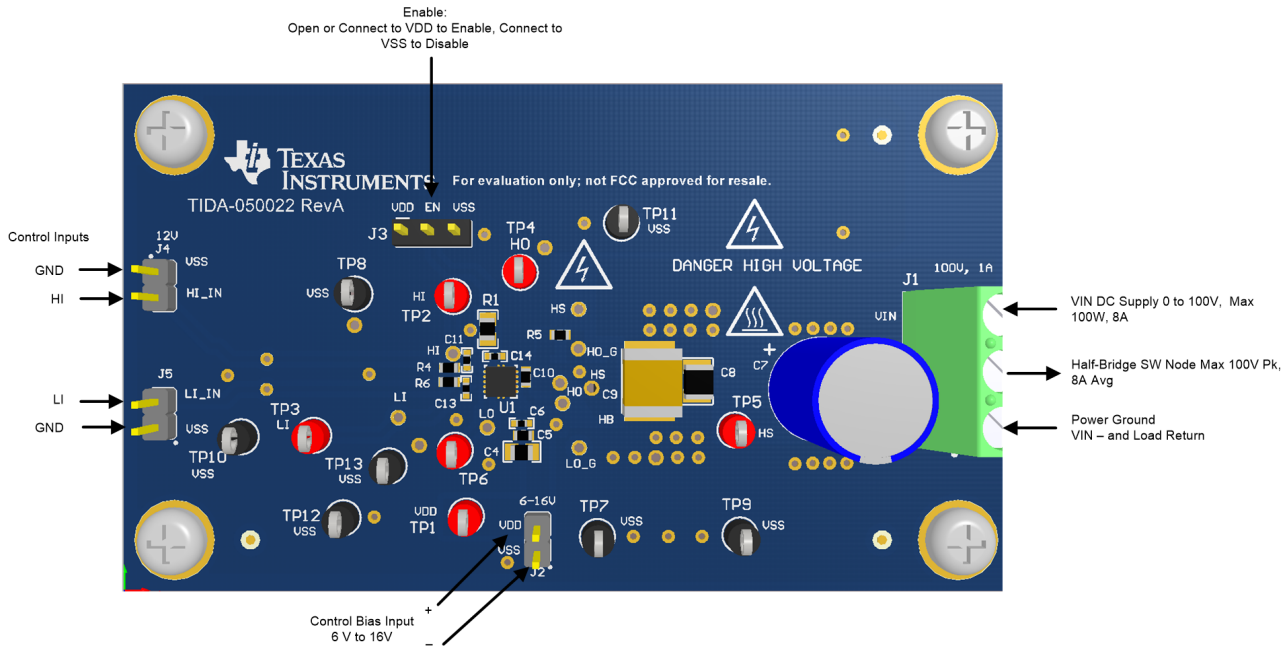
- DC voltage source: Capable of supplying the input of the board up to 100 V is desired; capable of supplying 10 A and supports current limiting
- DC bias source: Capable of 6-V to 18-V output at up to 0.3 A
- Oscilloscope: Capable of at least a 500-MHz operation, using oscilloscope probes with a "pigtail" spring ground clip instead of the standard alligator clip
- DC multimeters: Capable of 100-V measurement, suitable for determining operation and efficiency (if desired)
- DC load: Capable of 100-V operation at up to 10 A in constant current-mode operation
- Function generator
- Dual synchronous output for independent mode; capable of at least 0-V to 3-V signal.
- (Optional) Power meter: Capable of 100-V operation at up to 8 A

3.2 Testing and Results

3.2.1 Test Setup

Connect the input and bias supplies and DC electronic load as shown in Figure 6.

Figure 6. TIDA-050022 Top View



To obtain the best performance of this board:

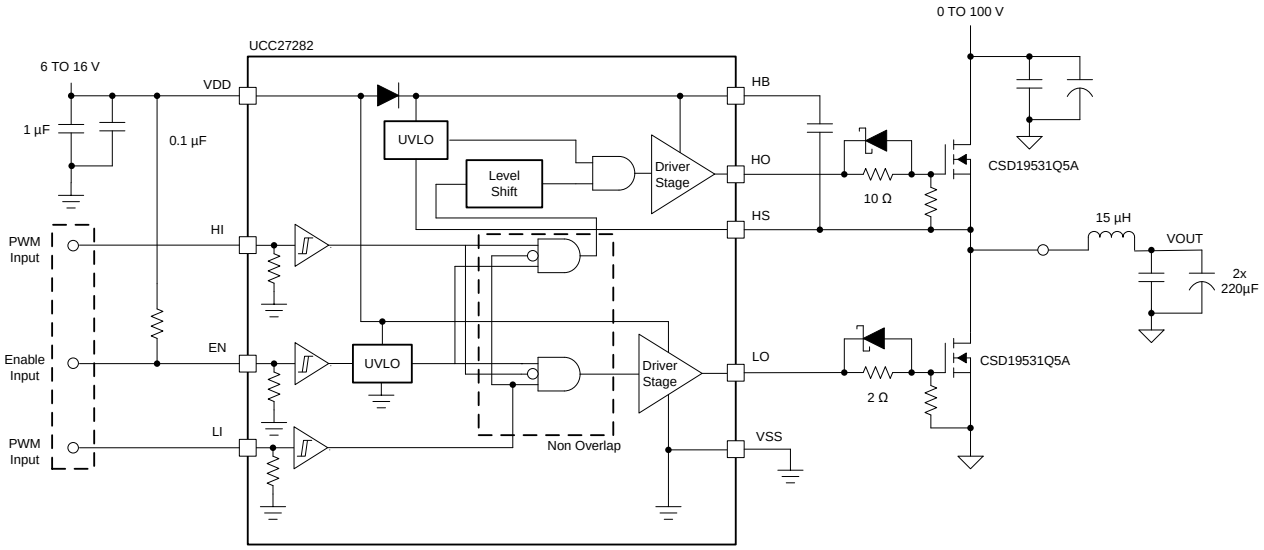
- Thermal: The parts used on this board are small with limited heatsink copper. If the dissipation exceeds 4 W, actively cool the board (as it has no heat-sink) using a fan or a similar device.
- Voltage spikes: As the test is running, whenever increasing the voltage and the current, it is important to monitor the voltage on the switched node to ensure the peak voltage does not exceed the 100-V rating of the CSD19531 FETs as this could damage the components.
- Additional capacitance on switched nodes: Typically, the method to observe the voltage at the high-side gate and the switched node is using a voltage probe. These probes come with several tens of pF of capacitance, which given the frequency can negatively impact efficiency. For precise efficiency measurements, remove all probes connected to switching nodes.

3.2.2 Test Results

3.2.2.1 Losses and Efficiency

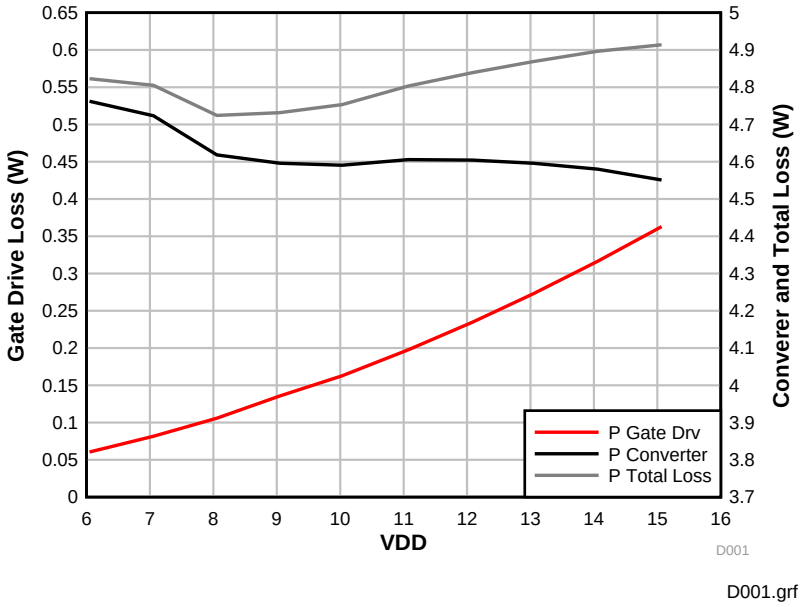
The TIDA-050022 power stage is tested in a synchronous-buck configuration to illustrate optimization of converter, gate drive and total losses. Figure 7 shows the tested configuration of the synchronous-buck converter operating under the following conditions: V_{IN} = 48 V, f_{SW} = 200 kHz and 300 kHz, I_{OUT} = 4 A(DC), LI/HI deadtime = 50 ns, 50 percent duty cycle.

Figure 7. TIDA-05022 Test Configuration



The synchronous-buck test circuit with CSD19531 MOSFETs loss data with an output power of 96 W and f_{SW} of 200 kHz is shown in Figure 8. You can see that the gate drive power dissipation increases with V_{DD} as expected. The power converter losses are higher at 6 V and 7 V and are relatively stable from 8 V and higher. The combined gate drive and converter losses are minimum at 8 V V_{DD}.

Figure 8. Gate Drive, Converter, and Total Loss: CSD19531 MOSFETs, and f_{SW} 200 kHz



In Table 2, the CSD19531 MOSFET parameters are compared to the CSD19533. Although the CSD19531 has lower $R_{DS(on)}$, the gate charge is higher and the body diode t_{RR} is longer than the CSD19533. Since the synchronous-buck test circuit will have continuous current operation and some body diode conduction, the body diode recovery time is an important consideration in this case. The synchronous-buck test data with the CSD19533 MOSFETs operating at 200 kHz is shown in Figure 9. You can see that the minimum total losses are still with V_{DD} = 8V and the converter and total losses are lower.

In Figure 10 the efficiency versus V_{DD} accounting for all losses is shown for the CSD19531 and CSD19533 MOSFETs. The CSD19533 efficiency is slightly higher in this test condition.

Figure 9. Gate Drive, Converter and Total Loss: CSD19533 MOSFETs, and f_{SW} 200 kHz

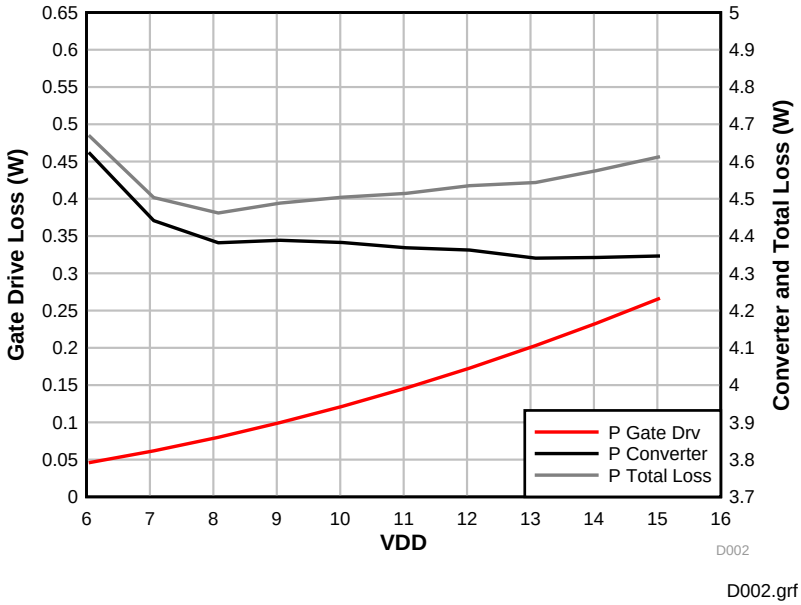
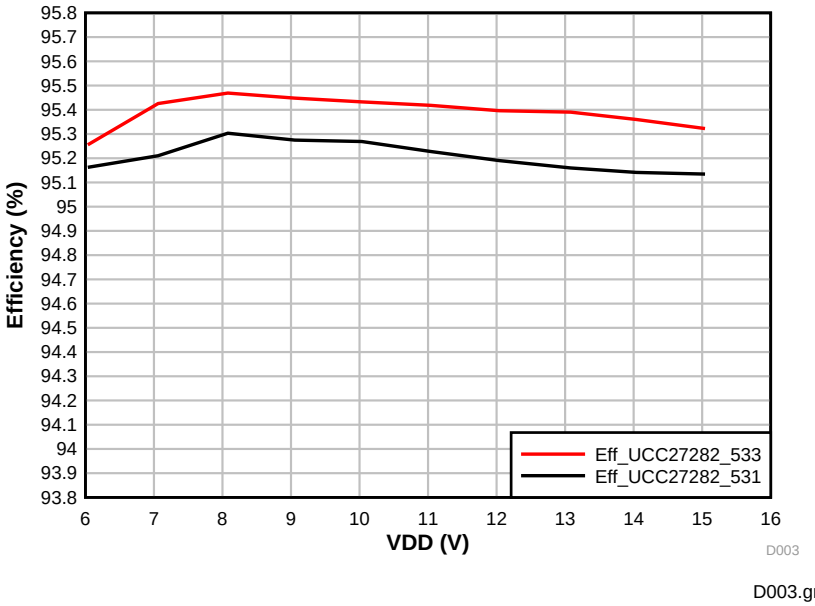


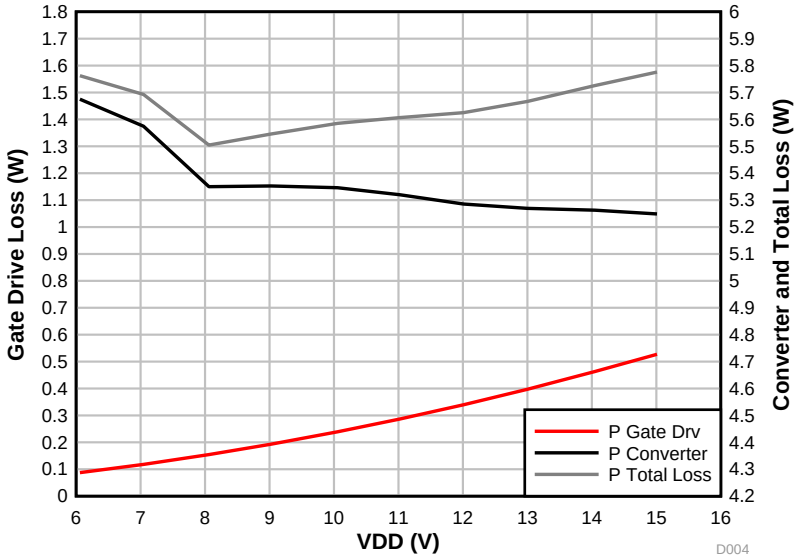
Figure 10. Efficiency versus V_{DD}: CSD19531 and CSD19533 MOSFETs, and f_{SW} 200 kHz



The converter was also tested at a switching frequency of 300 kHz to confirm if the optimum gate drive voltage follows the same trend.

The synchronous-buck test circuit with CSD19531 MOSFETs loss data with an output power of 96 W and f_{SW} of 300 kHz is shown in Figure 11. As before, the gate drive power dissipation increases with V_{DD} as expected. The power converter losses show the same trend and are higher at 6 V and 7 V and are relatively stable from 8 V and higher. The combined gate drive and converter losses are minimum at 8 V V_{DD}. Note that the overall losses are higher and the scale has increased.

Figure 11. Gate Drive, Converter, and Total Loss: CSD19531 MOSFETs, and f_{sw} 300 kHz



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With higher operating frequency the body diode recovery time will likely have more impact on the efficiency in the synchronous-buck converter. The synchronous-buck test data with the CSD19533 MOSFETs operating at 300 kHz in shown in Figure 12. You can see that the minimum total losses are still with V_{DD} = 8V and the losses are considerably lower.

In Figure 13, the efficiency versus V_{DD} accounting for all losses is shown for the CSD19531 and CSD19533 MOSFETs operating at 300 kHz. The CSD19533 efficiency is noticeably higher in this test condition.

Figure 12. Gate Drive, Converter and Total Loss: CSD19533 MOSFETs, and f_{sw} 300 kHz

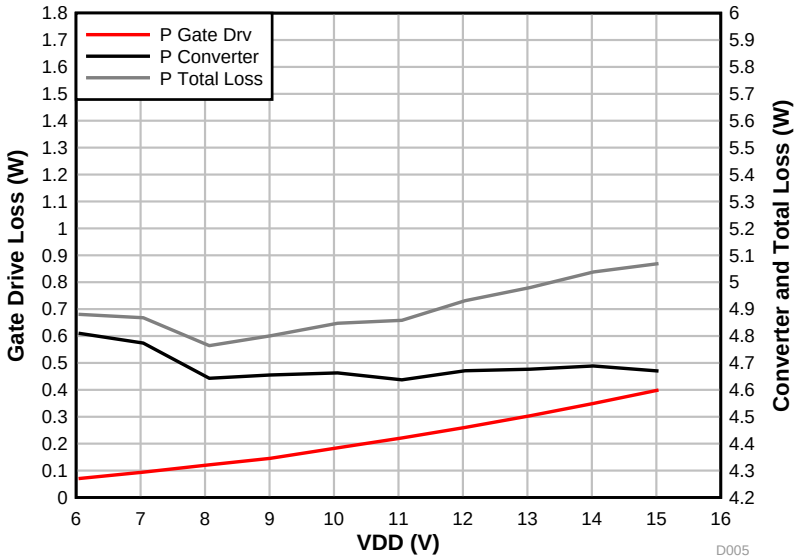

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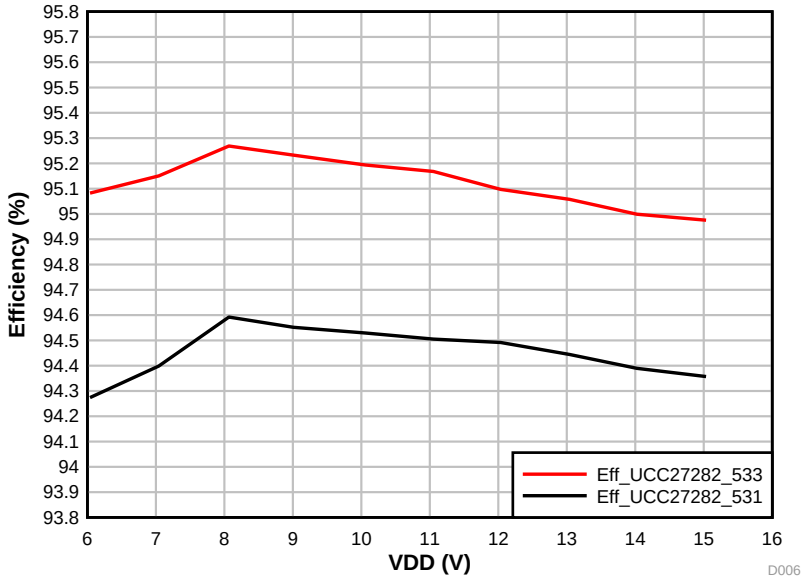
Figure 13. Efficiency Versus V_{DD}: CSD19531 and CSD19533 MOSFETs, and f_{SW} 300 kHz



3.2.2.2 Switching Waveforms

Figure 14 and Figure 15 show the CDS19531 low- and high-side gate turn off waveforms. Figure 16 shows the power stage switching at 200 kHz.

Figure 14. Low-Side Gate Turn Off: CSD19531

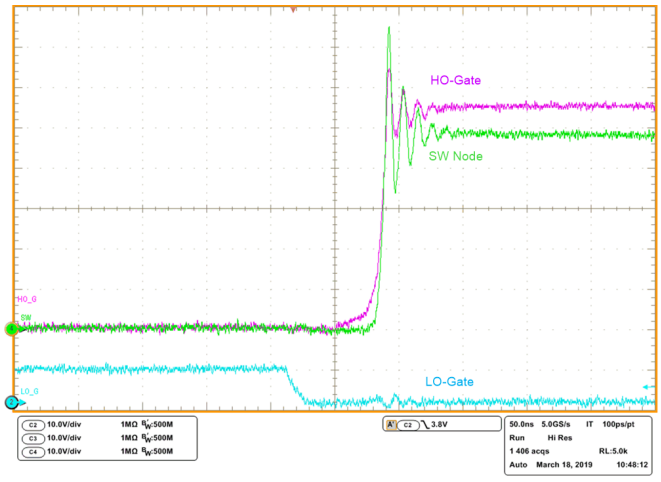


Figure 15. High-Side Gate Turn Off: CSD19531

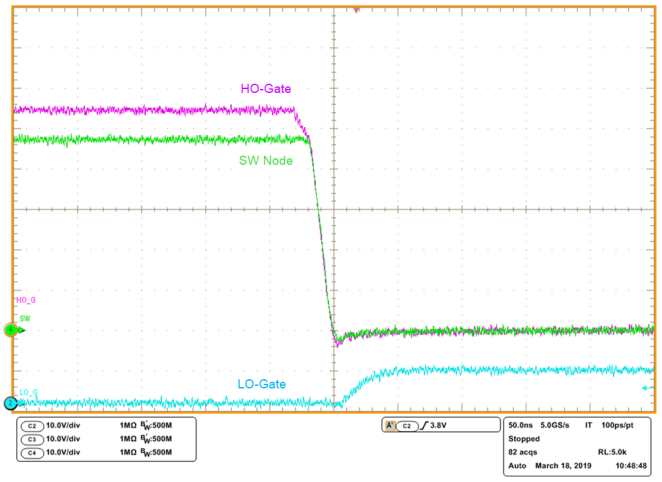
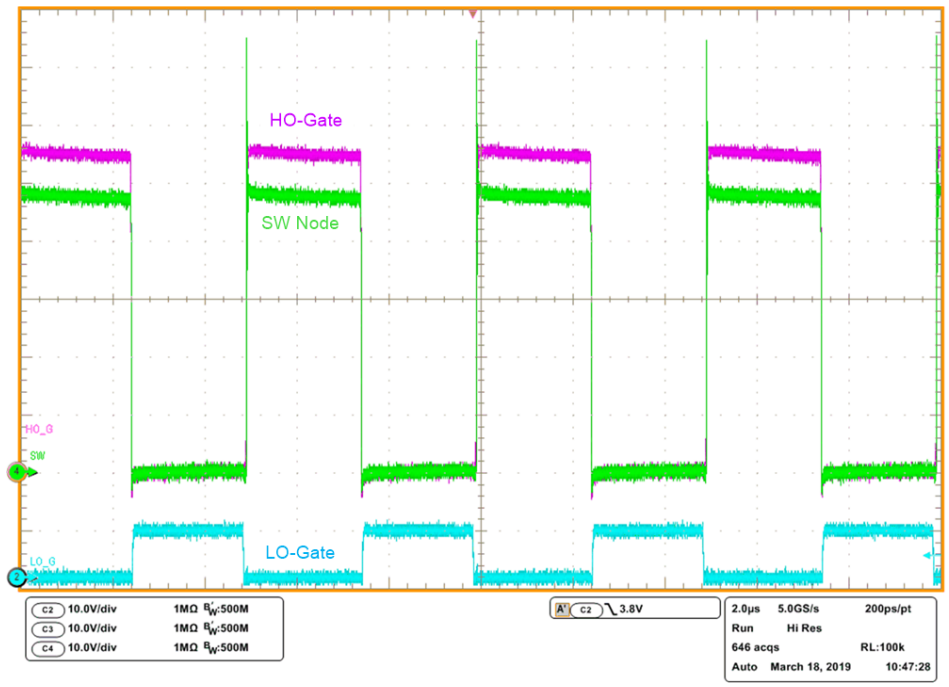


Figure 16. Power Stage Switching at 200 kHz: CSD19531



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050022.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050022.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050022.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-050022.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050022.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050022.

5 Related Documentation

1. Texas Instruments, *Using the UCC27282EVM-335 User's Guide*
2. Texas Instruments, *UCC27282 120-V Half-Bridge Driver with Cross Conduction Protection and Low Switching Loss* Data Sheet
3. Texas Instruments, *CSD19531Q5A 100 V N-Channel Nex FET™ Power MOSFETs* Data Sheet

5.1 Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2019) to A Revision	Page
• Changed link	15
• Changed link	15
• Changed link	15
• Changed link	15

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